

Michigan Technological University

EE 5900 04 - Spring 2001

Memory System Design & Simulation

webpage: http://www.ece.mtu.edu/faculty/btdavis/courses/mtu_5900_spr01

Course Description:

This course will examine the memory system or memory hierarchy of modern microprocessor systems. Primarily the focus will be on solid state memory devices and how the various technologies are used together to create the abstraction of a unified memory system. Also covered will be those functional units and structures in the microprocessor which directly interact with the memory system, or which are designed to tolerate the latency of the memory system. In addition, an architectural simulation tool - nominally SimpleScalar - will be used to explore the impact of changing the memory system upon the performance of the microprocessor system.

Instructor: Brian T. Davis

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Lectures - EERC 0226:

Monday, Wednesday, & Friday : 1pm - 2pm

Office Hours

Monday & Wednesday : 2pm - 3pm.

Thursday : 1-3pm

Note, will be in my office substantially more than the four hours listed above. You are welcome to stop by at your convenience, and under most circumstances I will take the time to handle your concern. However, under some situations I may ask that you come back during office hours or at a time which is mutually agreeable to us. If this policy is not acceptable, it is advised that you Email or Phone ahead to make an appointment during or outside of these times.

Required Text:

John L. Hennessy and David A. Patterson, "Computer Architecture : A Quantitative Approach - Second Edition." Morgan Kaufmann Publishers, 1995

Resource or Suggested Texts:

(1) Hill, Jouppi, and Sohi (Eds), "Readings in Computer Architecture." Morgan Kaufmann Publishers, 2000.

(2) Betty Prince, "High Performance Memories." John Wiley & Sons, 2000.

- (3) Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability." IEEE Press, 1997.
- (4) Selected Readings from Journals & Conferences which will be available on the course homepage.

Course Outline:

There will be two ongoing tracks of study during this semester. The first track will consist of coursework and readings. The required text (H&P) will be used for approximately the first 1/3 of the semester. We will be covering material on the memory functional units, virtual memory, and caches. The later 2/3 of the course will be occupied with reading papers from technical conferences and journals. These will be assigned a week in advance, and students are expected to come to class prepared to discuss the content.

The second track will cover usage of architectural simulation tools to examine the impact of changes in the memory hierarchy upon the performance of the microprocessor system. Regular programming assignments will be covered in lecture, and questions will be answered - however this will not be the focus of the lectures. The SimpleScalar simulation tool will be used, and covered, however if the students have the interest & initiative to use a different architectural simulation tool, the programs will be designed to be flexible enough that they could be completed with other software.

Lecture Topics:

- Processor System Architecture
- Processor Design for Memory Latency Tolerance
- Processor Computer Stratification
- Memory Hierarchy
- Solid State Memory Technologies
- Intelligent Memories
- Memory Controller Policies
- Simulation of Processor Systems
- Simulation of Memory Systems

Programming Content Outline:

- Introduction to SimpleScalar & Other Simulation tools
- Changing input parameters to SimpleScalar
- Adding parameters & statistics to SimpleScalar
- Integrating your own code into SimpleScalar
- Simulating a Unique Memory System Architecture using SimpleScalar

Attendance

Attendance will not be taken in this course, however it will count toward the class participation portion of the grade. If you feel that you have a legitimate reason for not attending any course session, if you let me know BEFORE the class session, via email, phone, or personal discussion, just about any excuse is likely to be favorably received. If you wait until AFTER the class session to see me about material covered in

your absence, or if you fail to see me about a missed class the absence is likely to negatively impact your class participation perception.

Evaluation/Grading

Grading will be highly subjective due to the small class size and nature of the class. Class participation will count for 15% of the final grade, and I expect students to arrive to class having read the assigned material. Failure to come to class prepared will result in a reduction in the class participation, and likely final grade.

The weighting of class components for final grades are as follows:

Exams (2)	20% each
Homework	10%
Class Participation	15%
Programming Assignments	35%

All exams/quizzes will be comprehensive and closed book/notes

Plagiarism and Cheating:

In the context of this class, plagiarism is defined as representing someone else's work as your own. Cheating is defined as violating stated rules for an exam or an assignment. Plagiarized work will receive a grade of F as will any assignment in which cheating occurred. If any student cooperation is allowed this will be explicitly spelled out in class or the assignments, otherwise no working in groups is allowed.