Michigan Technological University
EE 3173 - Fall 2004
Hardware/Software Systems Integration

webpage: ***http://www.ece.mtu.edu/faculty/btdavis/courses/mtu_ee3173_f04***

Course Description:

This course takes the knowledge from a number of prerequisite courses and integrates it into the basis of microprocessor based systems. EE3173 covers the integration of hardware and software into a complete system. EE3173 includes design and construction of I/O devices for microprocessor or microcontroller-based systems, communication and bus protocols, programming in assembler language and in "C", system integration and testing. EE3173 also covers the use and integration of FPGAs using both compiler driven digital design and HDL design tools. In the lab, knowledge gained in class will be used to implement and interface various I/O devices to FPGA and software based Nios development board.

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TA: TBD
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Lectures - EERC 229:

Monday, Wednesday & Friday: 2-3pm

Office Hours - EERC 729

Tue 2-3pm; Wed 3-4pm; Fri 1-2pm.

Note, I will be in my office substantially more than the three hours listed above. You are welcome to stop by at your convenience, and under most circumstances I will take the time to handle your concern. However, under some situations I may ask that you come back during office hours or at a time which is mutually agreeable to us. If this policy is not acceptable, it is advised that you Email or Phone ahead to make an appointment.

Required Text:

[Sta03] William Stallings, *Computer Organization and Architecture: Designing for Performance, 6th Ed.*, Prentice Hall, Upper Saddle River, NJ, 2000. ISBN: 0-13-035119-9
http://vig.prenhall.com/catalog/academic/product/1,4096,0130351199,00.html
http://williamstallings.com/COA6e.html

Resource or Suggested Texts:

[HP02] John L. Hennessy and David A. Patterson, “Computer Architecture : A Quantitative Approach - Third Edition.” Morgan Kaufmann Publishers, 2002. ISBN: 1-55860-724-2

[misc.] Selected Readings from Journals & Conferences which will be available through the course homepage.

Course Lecture Topics & Rough Outline:

- **Introduction**
  - Homepage & Syllabus Overview
- **Outline of NIOS system architectural features**
  - FPGAs /Altera Excalibur FPGA Development Board
  - Altera NIOS processor architecture & programming
  - Altera NIOS/Excalibur software development tools
- **Computer Evolution & Interconnection**
- **Microprocessor and microcontroller architectural issues**
  - Review and expansion on microprocessor architectures, pipelines, and I/O features
  - Microcontroller architectures, typical I/O devices and their applications in embedded systems
  - System level design of modern desktop Personal Computers
- **Memory Systems**
  - Internal Memory Systems
  - External Memory Systems
- **ISA characteristics**
  - RISC vs. CISC
  - IA-64 instruction set features
- **Principles and practice of I/O and communication including**
  - Bus signalling protocols,
  - Polled I/O, Programmed I/O, Direct Memory Access (DMA) and I/O Processors (I/O channels),
    - NIOS PIO port, keypad, & 7-segment LED display
    - NIOS interrupt handling w/ PIO port example
- **Typical I/O devices**
  - UARTS, SPIs
  - Principles of A/D & D/A conversion
  - Timers, applications, & PWM
    - Stepper motors
  - I/O Processors (Channels)
    - Case study: Intel 8089 IOP
- **Bus Architectures and operation**
  - Case studies of Various topologies
    - Board level Interconnect: ISA, PCI, PCI-X
    - Disk interconnect: SCSI, ATA
    - Serial port busses: RS-232, Firewire, USB
    - Real-time field busses (TTP/A vs. CAN)
    - Real-time safety-critical busses (TTP/C vs. Flexray)
- **Additional Topics to Be Determined…**

Goals

By the completion of the semester, students should be capable of:

1. Demonstrating familiarity and experience with System-On-a-Programmable Chip (SOPC) concepts and implementation in contemporary FPGA technology; including embedded processor cores, and selected industry standards for busses and I/O interfaces.
2. Demonstrating familiarity and experience using a contemporary design tools suite for hardware and software design and integration in an SOPC environment.
3. Demonstrating familiarity and experience in interfacing with a SOPC system with off-chip components, including A/D, D/A, amplification and fanout - using polled, interrupt driven and DMA I/O techniques.
4. Demonstrating familiarity and experience programming a processor embedded on an SOPC in both high level and assembly languages to monitor and control a real-world process, system, or device.

Laboratory Content Outline:

There will be approximately 12 labs to comprise the laboratory component of this course. These labs are changed each semester, but will almost certainly include:

- Nios Embedded Processor
- Nios software development & RS-232 communication
- Nios Assembly Language Programming
- Interrupt Driven I/O
- Interfacing the Nios system to A/D and D/A converters
- Stepper Motor Control
- Thermostat implementation
- Adding a DRAM controller to the Nios system
- Adding custom instructions to the Nios ISA
- DMA Driven I/O

Attendance

Attendance will not be taken in this course, however it will count toward the class participation portion of the grade. If you feel that you have a legitimate reason for not attending any course session, if you let me know BEFORE the class session, via email, phone, or personal discussion, just about any excuse is likely to be favorably received. If you wait until AFTER the class session to see me about material covered in your absence, or if you fail to see me about a missed class the absence is likely to negatively impact your class participation perception.

Evaluation/Grading

Grading will be highly subjective due to the small class size and nature of the class. Class participation will count for 5% of the final grade, and I expect students to arrive to class having read the assigned material. Failure to come to class prepared will result in a reduction in the class participation, and likely final grade.

The weighting of class components for final grades are as follows:

Prerequisite Exam	5%
Midterm Exams (2)	12% each
Final Exam	16%
Laboratory	40%
Quizzes	10% total
Class Participation	5%

All exams/quizzes will be comprehensive and closed book/notes, with no calculators of any sort allowed. Quizzes will be anounced in the class class before they are conducted.

Assignment questions & Late assignments

I will answer questions regarding assignments in office, lecture and via electronic forums. I will cease to respond to questions regarding an assignment 24 hours prior to that assignments due date. i.e. if an assignment is due Monday @ 4pm, ask your question PRIOR to Sunday @ 4pm or it will not be answered.

Late assignments - both homework and labs - will be penalized 20% for each M-F weekday that they are late. Exceptions to this rule will only be made for cases brought to the instructors attention PRIOR to the due date.

Plagiarism and Cheating:

In the context of this class, plagiarism is defined as representing someone else's work as your own. Cheating is defined as violating stated rules for an exam or an assignment. Plagiarized work will receive a grade of F, as will any assignment in which cheating occurred. If any student cooperation is allowed this will be explicitly spelled out in class or the assignments, otherwise no working in groups is allowed. Flagrant or repeated violations of this academic code of conduct will result in a grade of F assigned for the course.