

All homework in this course should be done individually. Violation of this rule may result in a zero grade being assigned for the homework, or if flagrant or repeated an F for the course. It is necessary to provide citations or URLs for all questions when information from sources other than the course materials has been utilized.

**From the Stallings 6th Edition Text**

- 1). Problem 7.5
- 2). Problem 7.7

**From the Web: Bus technologies**

Provide URLs as citations.

- 3). Generate a table, which includes as a column each of the bulleted bus technologies, and a row for each of the characteristics given below.
  - USB
  - Firewire
  - Hypertransport
  - a) Application area
  - b) Bandwidth
  - c) Signalling technology
  - d) Signalling voltage
  - e) Number of interrupting devices supported
  - f) Number of signals required (estimates may be required)
  - g) URL specific to Bus where the best info on this bus can be found

Find a datasheet in PDF, and provide a URL for:

- 4). Interrupt controller, other than the 8259.
  - a) How many interrupt sources are supported?
  - b) How is the interrupt source or vector encoded?
- 5). DAC other than MAX525
  - a) What is the total address space of the I/O Module
  - b) What is the maximum frequency of the DAC
  - c) What is the number of bits of precision provided by the MAX525
- 6). DMA Controller, other than the 8089.
  - a) How many channels are supported?
  - b) What is the address space of the DMAC?

## Related Material

7). I/O Performance. Compare and graph the overhead involved in Interrupt vs. Polled I/O with realistic values. The I/O device being examined is a Hard-Drive which has a maximum throughput rate of 36.29 MB/s. The microprocessor being examined is assumed to have a 50MHz clock frequency. Assume that the three I/O synchronization mechanisms being compared are:

- Polled I/O - Has a transfer granularity of 128 bytes / transfer. The polling routine takes 800 cycles when there is data present, and 250 cycles when no data is present.
- Interrupt I/O - Has a transfer granularity of 256 bytes / transfer. The interrupt handling routine requires 1650 cycles to execute.
- DMA I/O - Has a transfer granularity of 128Kbytes. The initialization of a DMA transfer requires 1200 cycles, the finalization of a DMA transfer requires 600 cycles. You may ignore bus contention in your calculations.

Now, consider the overhead of each of these systems, if the fraction of the throughput of the device which is being utilized is 100%, 80%, 50%, 25%, 5%. Your data should be presented in a table, where the rows are the percentages, and the columns are the I/O mechanisms. This is convenient to do in Excel or an equivalent spreadsheet. Graph your table, submit the graph with your solutions. When discussing all three I/O mechanisms - is it possible to find a synchronization mechanism which is the consistent (in all cases) best performer? Is it possible to find a consistent worst performer?

## Definitions

Provide a Definition for the following Terms

- 8). Firewire, USB, Hypertransport
- 9). What is the function of an Intel 8259
- 10). What is the function of an Intel 8089
- 11). Eye diagram
- 12). CRC
- 13). I/O Channel
- 14). I/O Processor - how is it different than a CPU