

All homework in this course should be done individually. Violation of this rule may result in a zero grade being assigned for the homework, or if flagrant or repeated an F for the course.

- 1). In the design of a motherboard using a conventional North & South bridge arrangement, it is desired that there be 6.4GB/s of bandwidth in each direction between the CPU and the northbridge, and only 1.6GB/s of bandwidth in each direction between the northbridge and the southbridge. If the Hypertransport protocol is being used for interconnection between components, how many signal pins would be required for each component link.

- 2). Assuming the following sequence of reads & writes to 3 unique banks of a Micron MT48LC8M16A2-7E SDR SDRAM, draw a timing diagram and calculate the # of cycles required to complete all accesses from the precharge of the first active page to the last data cycle. Provide timing for each event & show all work.
WRITE: Bank 0, Page 0x10
READ: Bank 0, Page 0x10
READ: Bank 1, Page 0x20
WRITE: Bank 2, Page 0x30
READ: Bank 0, Page 0x10

- 3). The DRAM memory system of an embedded computer is designed using 256 Mbit memory chips. The bus width of the system is 64 bits. Draw a diagram and show the minimum number of devices for each of the following device configurations.
 - a) 64M x4
 - b) 32M x8
 - c) 16M x16

- 4). Draw a diagram of one possible arrangement between a processor BIU and a number of Micron 8Mb flow-through ZBT SDR SRAM which allows for 64-bit bus and 8MBytes total memory size. If the I/O voltage is 2.5v, what is the part # of the SRAM used in your diagram? What is the theoretical bandwidth of this interface?

- 5). In the design of a computer memory hierarchy there are a number of levels. Each level has its own characteristic and thus approach for dividing the address bits. Assuming a 32-bit CPU with each of the levels below with associated characteristics.
- L1: 16 KByte, 2-way set associative, 32 Byte line size
 - L2: 256 KByte, 4-way set associative, 64 Byte line size
 - DRAM: 256 MBytes, one DIMM comprised of 8 Micron 256Mb SDR SDRAM: MT48LC32M8A2 devices
- Specify what range of bits correspond to: tag, index, bank or byte at each of these levels. Similarly, assuming this system uses Virtual Memory specify the range of bits corresponding to the VPN, PPN and byte.
- VM: 40-bit virtual address and a 32-bit physical address
- 6). If a direct-mapped cache size of 32KB is required to achieve the average access time target of the L1 cache, and the operating system has defined a page size of 512 bytes, what associativity is required so that the cache can be indexed using the page offset bits of the virtual address? If you could change the page size but direct-mapped cache was a firm requirement, what page size would you pick?
- 7). Write a generalized average access time (AAT) equation for the following memory hierarchy using the symbolic names given in parenthesis?
- L1 cache (L1_latency, L1_miss_rate)
 - L1 cache victim cache (VC_latency, VC_miss_rate)
 - L2 cache (L2_latency, L2_miss_rate)
 - Main memory (mem_latency)
- It is known that you will have to make some additional assumptions about the sequencing and policies of the caches. State all assumptions
- 8). Generate a table which shows each of the following characteristics
- Clock frequency
 - Bandwidth
 - Best case access latency
 - Worst case access latency
 - Minimal total memory capacity assuming a 64-bit wide bus

For each of the following memory devices.

- a) DDR SRAM (Micron 36Mb DDRII CIO SRAM: MT57W4MH8J-4)
 - b) EDO DRAM (Micron 64Mb: MT4LC4M16R6-5)
 - c) SDR SDRAM (Micron 256Mb: MT48LC64M4A2-7E)
 - d) DDR SDRAM (Micron 512Mb: MT46V128M4-75)
- 9). WEB SEARCH: Examine the pin interfaces of the following memory devices. Determine, of the connected pins, how many are dedicated to power, data, address & other.
- a) Cypress Asynchronous SRAM: CY7C1061AV33
 - b) Cypress Synchronous Flow-through SRAM: CY7C1441V33
 - c) Infineon SDR SDRAM: HYB 39S512400AT-7
 - d) Infineon DDR SDRAM: HYB25D512160AT-8
 - e) Samsung DDR2: K4T51083QM-GCD4
- Please provide citations/URLs
- 10). After examining the data for the Infineon DDR2 device above, generate a table which has as rows each of the speed grades available {PC200, PC266A & PC333} and shows the CL, tRP, tRCD and the sum of all three in nanoSeconds.

Provide a Definition for the following Terms

- 11). BIU
- 12). CMP & SMT. How are they alike, how are they different?
- 13). North Bridge
- 14). Front-Side-Bus
- 15). HyperTransport
- 16). PCI-X
- 17). Flow-Through
- 18). Pipelined SRAM
- 19). ZBT
- 20). DRAM Page
- 21). ECC