

All homework in this course is intended to be done individually.

- 1). Assume all the SRAM devices given below have a capacity of 1 Mbits.
 - a) If a x16 device has 2048 word-lines, how many bit-lines are necessary?
 - b) If a x16 device has 2048 word-lines, how many bits are input to the column decoder?
 - c) If a x8 device has 256 bit-lines, how many word-lines are necessary?
 - d) If a device has 512 word-lines, 2048 bit-lines, and 6 bits input to the column decoder, what is the output width (i.e. x4, x16, x32, etc.) of the device?
 - e) Which of the above devices would you anticipate to have the lowest access latency, and why?
 - f) Which of the above devices would you anticipate to have the highest bit-density, and why?
- 2). Array Organization: complete table where it is possible.

Capacity	Data bits out	Row Address bits	Word lines	Column Address Bits	Bit Lines
64 Kbit	x8	8	256		
128 Kbit	x8	7		7	
256 Kbit	x16			5	512

Assuming a common technology for all devices, which device would you assume to have the lowest access latency?

- 3). Interface characteristics: complete the table where it is possible.

	Data bits out	Frequency	Clock Cycles	Access Latency	Theoretical Bandwidth
Asynchronous SRAM	x16	n/a	n/a	20nS	
Flow-Through SRAM	x32	100 MHz			400MB/s
Pipelined SRAM	x32	250 MHz		12nS	

- 4). Assuming the following sequence of reads & writes to 3 unique banks of a Samsung K7D163674B DDR SDRAM, draw a timing diagram and calculate the # of cycles required to complete all accesses from the precharge of the first active page to the last data cycle. The datasheet is found below: <http://www.samsung.com/Products/Semiconductor/HighSpeedSRAM/index.htm>. Provide timing for each event & show all work.
- WRITE: Bank 0, Page 0x10
 READ: Bank 0, Page 0x10
 READ: Bank 1, Page 0x20
 WRITE: Bank 2, Page 0x30
 READ: Bank 0, Page 0x10
- 5). The DRAM memory system of an embedded computer is designed using 256 Mbit memory chips. The bus width of the system is 64 bits. Draw a diagram and show the minimum number of devices for each of the following device configurations.
- 64M x4
 - 32M x8
 - 16M x16
- 6). Describe the differences between the functional block diagrams of an asynchronous SRAM and the functional block diagram of a synchronous SRAM. What functional blocks are unique to one or the other? What changes are necessary in the core memory array(s)?
- 7). Micron recommends that QDR SRAM be used when the read:write ratio is 2:1 or less, and DDR SRAM be used when the read:write ratio is 2:1 or more. Explain why Micron makes this recommendation. What are the relevant differences between these two devices?
- 8). In the context of moving from an Asynchronous SRAM interface to a Synchronous SRAM interface, provide the PROs and CONS of the Synchronous interface.

Provide a Definition for the following Terms

- North Bridge
- Front-Side-Bus
- HyperTransport
- Flow-Through
- Pipelined SRAM
- ZBT
- DDR & DDRII
- QDR, QDRII & QDRIII+