

Michigan Technological University

EE 5752- Spring 2005

Digital Storage Technologies

webpage: http://www.ece.mtu.edu/faculty/btdavis/courses/mtu_ee5752_s05/

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Course Description:

This course will examine digital storage technologies used in modern microprocessor based workstations. A variety of products are used for storage and memory in the memory hierarchy of modern workstations including solid-state memories, magnetic and optical disks. The examination of solid state memory devices will illustrate how the various technologies are used together to create the abstraction of a unified memory system. This examination will include the differentiating characteristics of the devices and interfaces available, as well as simulation of a memory hierarchy encompassing many of these technologies. The discussion of magnetic and optical disks will be an academic examination of the state of the art in these devices. Also covered will be those functional units and structures in the microprocessor which directly interact with the memory system, or which are designed to tolerate the latency of the memory system. In addition, an architectural simulation tool - nominally SimpleScalar - will be used to explore the impact of changing the memory system upon the performance of the microprocessor system.

Lectures - EERC 227:

Monday, Wednesday & Friday: 10-11 am

Office Hours - EERC 729

Monday & Friday : 11-11:50am, Tuesday 2-3pm

Note, will be in my office substantially more than the hours listed above. You are welcome to stop by at your convenience, and under most circumstances I will take the time to handle your concern. However, under some situations I may ask that you come back during office hours or at a time which is mutually agreeable to us. If this policy is not acceptable, it is advised that you Email or Phone ahead to make an appointment during or outside of these times.

Required Text:

Betty Prince, "High Performance Memories." John Wiley & Sons, 2000.

Resource or Suggested Texts:

- (1) Hill, Jouppi, and Sohi (Eds), "Readings in Computer Architecture." Morgan Kaufmann Publishers, 2000.
- (2) John L. Hennessy and David A. Patterson, "Computer Architecture : A Quantitative Approach - Third Edition." Morgan Kaufmann Publishers, 2002
- (3) Ashok K. Sharma, "Semiconductor Memories: Technology, Testing, and Reliability." IEEE Press, 1997.
- (4) Selected Readings from Journals & Conferences which will be available on the course homepage.

Course Outline:

The coursework will consist of readings, homeworks, programming assignments and exams. The readings will be from a variety of sources, available primarily through the course homepage and the required textbook. We will begin by covering the processor memory functional units, virtual memory, caches and bus interconnections. Then we will use the required text for discussion of solid state memory. The later portions of the course will be occupied with reading papers from technical conferences and journals. All readings will be assigned a week in advance, and students are expected to come to class prepared to discuss the content.

A concurrent track of study will cover usage of architectural simulation tools to examine the impact of changes in the memory hierarchy upon the performance of the microprocessor system. Regular programming assignments will be covered in lecture, and questions will be answered - however this will not be the focus of the lectures. The SimpleScalar simulation tool will be used, and covered. However if the students have the interest & initiative to use a different architectural simulation tool, the programs will be designed to be flexible enough that they could be completed with other software.

Goals

By the completion of the semester, students should:

- Understand the construction, usage and characteristics of each of the following memory technologies
 - SRAM, DRAM, Flash, MagRAM, NVRAM, and other solid state devices
 - Magnetic & Optical Disks
- Be able to describe appropriate usage of each of the covered memory technologies in the memory hierarchy of a conventional microprocessor-based system.
- Be able to describe available controller policies for each memory technology, as well as the utility and distinguishing attributes of the controller policies.
- Have experience with at least one architectural simulation tool capable of memory hierarchy investigations.

Lecture Topics:

- Processor System Architecture
 - Bus Interconnections
 - Processor Design for Memory Latency Tolerance
 - Memory Hierarchy

- Solid State Memory Technologies
 - SRAM
 - Flash
 - DRAM
- Memory Controller Policies
- Future Memory Technologies
 - Intelligent Memories
 - Magnetic RAM
- Storage Systems
 - Magnetic Disks
 - Optical Disks
- Simulation of Processor Systems
- Simulation of Memory Systems

Programming Content Outline:

- Introduction to SimpleScalar & Other Simulation tools
- Changing input parameters to SimpleScalar
- Adding parameters & statistics to SimpleScalar
- Integrating your own code into SimpleScalar
- Simulating a Unique Memory System Architecture using SimpleScalar

Attendance

Attendance will not be taken in this course, however it will count toward the class participation portion of the grade. If you feel that you have a legitimate reason for not attending any course session, if you let me know BEFORE the class session, via email, phone, or personal discussion, just about any excuse is likely to be favorably received. If you wait until AFTER the class session to see me about material covered in your absence, or if you fail to see me about a missed class the absence is likely to negatively impact your class participation perception.

Evaluation/Grading

Grading will be highly subjective due to the small class size and nature of the class. Class participation will count for 10% of the final grade, and I expect students to arrive to class having read the assigned material. Failure to come to class prepared will result in a reduction in the class participation, and likely final grade.

The weighting of class components for final grades are as follows:

Midterm Exams (2)	15% each
Final Exam	20%
Programming Assignments	30%
Quizzes/Homework	10%
Class Participation	10%

All exams/quizzes will be comprehensive and closed book/notes

Plagiarism and Cheating:

In the context of this class, plagiarism is defined as representing someone else's work as your own. Cheating is defined as violating stated rules for an exam or an assignment. Plagiarized work will receive a grade of F as will any assignment in which cheating occurred. When in question, always cite a source used for reference in a homework, report or programming assignment. If any student cooperation is allowed this will be explicitly spelled out in class or the assignments, otherwise no working in groups is allowed.