

All homework in this course is intended to be done individually.

- 1). The memory hierarchy of a modern workstation appears to be a single unified address space to the program. Explain why the memory hierarchy of a modern workstation - with many levels and complexities - is constructed in a complex pyramid encompassing multiple memory technologies.
- 2). Provide (3) goals of virtual memory.
- 3). What is meant by “hitting a wall” as it is described in [McKee95]. Do you think that this technological wall has been overcome? Why or why not? Do you see any imminent “walls” limiting the performance of microprocessor systems?
- 4). Suppose that you have a two-level cache, L1, and L2. The hit rate for the L1 cache is 95% and the hit rate for the L2 cache is 80%. A memory reference which hits in the L1 cache takes 1 cycle, a memory reference which misses in L1 but hits in L2 takes 8 cycles, and a reference which misses in both and accesses DRAM takes 120 cycles. What is the average memory access time, assume that accesses to the three memory levels are strictly serial?
- 5). Locality
 - a) Describe in words, or with pseudo-code, a program that would exhibit a high degree of temporal locality, but relatively little spatial locality, with respect to its data references.
 - b) Describe in words, or with pseudo-code, a program that would exhibit a high degree of spatial locality, but very little temporal locality, with respect to its data references.
- 6). The following is a string of accesses to a direct mapped L1 cache with a 16 byte linesize and 32 lines. Classify each access as a Hit or one of the four following types of misses: Compulsory, Capacity, Conflict or Coherence.

0x000	0x208
0x008	0x090
0x080	0x080
0x200	0x480
0x008	0x088

- 7). Some cache enhancements are more appropriate to either I or D side accesses. For each of the following state whether they are effective for I, D or Both and justify your answer.
- a) Non-Blocking
 - b) Stream Buffer
 - c) Trace Cache
- 8). Web search
- a) Describe only the on-chip memory hierarchy (levels of cache, associativity, size, linesize [if you can find it] for each cache) for the following processors:
Alpha 21264
Pentium 4(Northwood)
Athlon (Thoroughbred)
Itanium
 - b) Describe the distinguishing features of the memory hierarchy for the following:
Cray C90
Unisys ES7000
Please provide citations/URLs
- 9). Explain the differences between the following types of memory, and the name which could be given to these devices as a class.
ROM, PROM, EPROM, EEPROM, Flash

Provide a Definition for the following Terms

- 10). Memory Hierarchy
- 11). Temporal Locality
- 12). Spatial Locality
- 13). Split Cache
- 14). Basic Block
- 15). Victim Cache
- 16). MSHR
- 17). Trace Cache
- 18). Register Update Unit