

All homework in this course is intended to be done individually.

- 1). The case has been made that cache inclusion is automatically maintained in a two-level cache hierarchy, where L1 is closer to the processor than L2, iff $a_2 \geq a_1$ and $b_2 \geq b_1$, where a_n is the associativity of cache level n , and b_n is the block size of cache level. For this statement to hold true, what else must be true of the controller and replacement policy of these caches.
- 2). Explain how it is possible for memory accesses to appear at the DRAM controller “out-of-order” when compared to the sequential program ordering. What functional units are necessary in the processor for this to occur, and what role do they play?
- 3). Explain why differential signalling has become more popular in communication interfaces between discrete components such as the processor and chipset, or elements of the chipset.
- 4). Explain the motivation for the multiple tools included with the SimpleScalar 3.0d simulation package. Why is sim-outorder not uniquely sufficient?
- 5). Assume all the SRAM devices given below have a capacity of 1 Mbits.
 - a) If a x16 device has 2048 word-lines, how many bit-lines are necessary?
 - b) If a x16 device has 2048 word-lines, how many bits are input to the column decoder?
 - c) If a x8 device has 256 bit-lines, how many word-lines are necessary?
 - d) If a device has 512 word-lines, 2048 bit-lines, and 6 bits input to the column decoder, what is the output width (i.e. x4, x16, x32, etc.) of the device?
 - e) Which of the above devices would you anticipate to have the lowest access latency, and why?
 - f) Which of the above devices would you anticipate to have the highest bit-density, and why?
- 6). A given x32 Asynchronous SRAM device has a access latency of 20nS, what is the bandwidth of this device?
- 7). Locate the datasheet for the IBM IBM0436166XLAC SRAM device, and determine the Latency to the first word, and the bandwidth of this device.

Provide a Definition for the following Terms

- 8). Non-Volatile Memory
- 9). Register Update Unit
- 10). RAW, WAW, WAR Hazard
- 11). Aspect Ratio
- 12). Bit Line
- 13). Word Line
- 14). Non-Uniform Access Latency
- 15). ZBT, SDR, DDR, QDR
- 16). SRAM Compiler