

All homework in this course should be done individually. Violation of this rule may result in a zero grade being assigned for the homework, or if flagrant or repeated an F for the course.

- 1). Draw a diagram of one possible arrangement between a processor BIU and a number of IBM 0436A8ACLAB - 50 ZBT SDR SRAM which allows for 64-bit bus and 8MBytes total memory size. What is the theoretical bandwidth of this interface?
  
- 2). Assuming the following sequence of reads & writes to 3 unique banks of a Micron MT48LC16M16A2-7E SDR SDRAM, draw a timing diagram and calculate the # of cycles required to complete all accesses from the precharge of the first active page to the last data cycle. Provide timing for each event & show all work.  
WRITE: Bank 0, Page 0x10  
READ: Bank 0, Page 0x10  
READ: Bank 1, Page 0x20  
WRITE: Bank 2, Page 0x30  
READ: Bank 0, Page 0x10
  
- 3). The DRAM memory system of an embedded computer is designed using 128 Mbit memory chips. The bus width of the system is 64 bits. Draw a diagram and determine the minimum number of devices for each of the following device configurations, the minimum capacity of this configuration & therefor the granularity of memory added.
  - a) 32M x4
  - b) 16M x8
  - c) 8M x16
  
- 4). Generate a table which shows each of the following characteristics
  - a) Clock frequency
  - b) Bandwidth
  - c) Best case access latency
  - d) Worst case access latency
  - e) Minimal total memory capacity assuming a 64-bit wide bus

For each of the following memory devices.

- a) EDO DRAM (Micron 64Mb: MT4LC4M16R6-5)
- b) SDR SDRAM (Micron 256Mb: MT48LC64M4A2-7E)
- c) DDR SDRAM (Micron 512Mb: MT46V128M4-75)

5). WEB SEARCH: Examine the pin interfaces of the following memory devices. Determine, of the connected pins, how many are dedicated to power, data, address & other.

- a) Cypress Asynchronous SRAM: CY7C1061AV33
- b) Cypress Synchronous Flow-through SRAM: CY7C1441V33
- c) Infineon SDR SDRAM: HYB 39S512400AT-7
- d) Infineon DDR SDRAM: HYB25D512160AT-8
- e) Infineon DDR2 SDRAM: HYB18T1G800AF-3.7
- f) Samsung DDR2: K4T51083QM-GCD4

Please provide citations/URLs

6). After examining the data for the Infineon DDR2 device datasheet above, generate a table which has as rows each of the speed grades available {DDR2-400 and DDR2-533} and shows the CL, tRP, tRCD and the sum of all three in nanoSeconds.

Provide a Definition for the following Terms

- 7). BIU
- 8). CMP & SMT. How are they alike, how are they different?
- 9). North Bridge
- 10). Front-Side-Bus
- 11). Flow-Through
- 12). Pipelined SRAM
- 13). ZBT
- 14). DRAM Page
- 15). ECC