

University of Toledo

EECS 416 - Microcomputer Systems I

Instructor : Brian T. Davis
email : bdavis@eecs.utoledo.edu
Office : 2040 Nitschke
Phone # : 419-530-8171 (Tue/Thur)
Phone # : 313-764-8033 (M/W/F)

TA : Joel Anaple
email : janaple@eecs.utoledo.edu

Office Hours

Brian : Tuesday 11 am - 12:30 pm & Thursday 4pm-5:30 pm

Lectures:

Tuesday & Thursday 2pm - 3:40pm

Labs:

LAB 1 : Tuesday 4pm-6:30pm	Brian
LAB 2 : Wednesday 8am -11:30am	Joel
LAB 3 : Thursday 10am-12:30 pm	Brian
LAB 4 : Friday 10am-12:30 pm	Joel

Webpage:

<http://www.eecs.utoledo.edu/~bdavis/>

Required Text:

Barry B. Brey, "The Intel Microprocessors 8086/8088, 80186, 80286, and 80486: Architecture Programming and Interfacing", Prentice Hall, Third Edition, 1995.

Suggested Texts:

- (1) Harold S. Stone, "Microcomputer Interfacing", Addison-Wesley, 1982.
- (2) Yu-cheng Liu & Glenn A. Gibson, "Microcomputer Systems: The 8086/8088 Family Architecture, Programming and Design", Prentice Hall, Second Edition, 1986.
- (3) "8086/8088 User's Manual: Programmer's and Hardware Reference", Intel, 1989, Order # 240487-001.
- (4) "iAPX 86/88, 186/188 User's Manual: Programmers Reference", Intel, 1986, Order # 210911-003.

Course Outline:

The course will cover the architecture of the Intel 80186 microprocessor, including some comparisons between this and other members of the x86 family. This processor will be approached with dual intent. First, the ability to program in assembly for this processor, including knowledge of the internal registers, processor status flags, addressing modes, instruction set, and the use of stacks in procedures and interrupt handlers. Second, how to interface the 80186 into a simple microcomputer system containing read-only memory, read-write memory, input and output devices and interrupt sources. Topics pertinent to these goals will also be covered together with alternative methods not applicable to the 80186 processor.

Lecture Topics:

- The 80186 Microprocessor
 - Programmers view of the architecture
 - Hardware Architecture
- Busses - The language of processors (Local Bus, ISA, EISA, PCI)
- Memory Architecture (DRAM, SRAM, SDRAM, RamBus)
- I/O interfaces - polled I/O, interrupt I/O
- Interrupts, interrupt handlers & device drivers
- Serial I/O
- Disk Subsystem - Disk Busses (IDE, EIDE, SCSI) and disk timings
- Advanced Microprocessors (time allowing) - Pentium, Pentium Pro, Klamath, AMD K5, Cyrix M2

Laboratory Topics:

- Introduction to the HP Development System - strictly programming
- Programming and interfacing to a EPROM - Chip Select Unit
- Parallel I/O
- Using Timers to generate a waveform
- Writing a Interrupt handler for asynchronous I/O
- Using the 80186 DMA Controllers
- Using Serial I/O

Evaluation/Grading

Midterm	20%
Final Exam	20%
Homework/Quizzes	20%
Lab Assignments	25%
Final Lab Project	15%

All exams/quizzes will be comprehensive and closed book/notes