

## CURRICULUM VITAE

November, 2005

# Brian T. Davis

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Assistant Professor  
Michigan Tech  
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## Academic Background

- 2001      Ph.D.      Computer Science & Engineering, University of Michigan - Ann Arbor,  
Dissertation title: Modern DRAM Architectures
- 1994      M.S.E.      Computer Science & Engineering, University of Michigan - Ann Arbor,  
Areas of Emphasis: Digital Arithmetic and Hardware Description Languages
- 1991      B.S.E.E.      Electrical Engineering, Michigan Technological University,  
*Magna Cum Laude*, Computer Option, Thematic: Psychology

## Research Interests

- Application of static and dynamic access control protocols on Synchronous DRAM
- Address mappings in the microprocessor system memory hierarchy
- Hardware description languages for prototyping and reconfigurable computing
- Development of embedded systems for unattended environmental monitoring

## Academic, Teaching & Professional Experience

- 2001 -              Assistant Professor, Department of Electrical & Computer Engineering,  
Michigan Tech, Houghton MI
- 1998 - 2000      Graduate Student Research Assistant, Advanced Computer Architecture Lab,  
University of Michigan, Ann Arbor MI
- 1997-1998      Adjunct Professor, Department of Computer Science, Willamette University,  
Salem OR
- 1997              Visiting Lecturer, Department of Electrical Engineering, University of  
Toledo, Toledo OH
- 1994 - 1997      Graduate Student Research Assistant, Advanced Computer Architecture Lab,  
University of Michigan, Ann Arbor MI
- 1986 - 1994      Recurring employment with General Motors, both direct and as a contract  
employee, during high-school, college summers, and between undergrad and  
graduate work, responsibilities including tasks such as CAD station operator  
for plant layout, anthropomorphic text device (crash-test dummy) calibration,  
onboard data acquisition instrument programming, and powertrain control  
module programming.

## Professional Honors

Michigan Tech distinguished teaching award winner, 2004-2005 Academic Year  
Finalist for the Michigan Tech distinguished teaching award, Michigan Tech  
Academy of Teaching Excellence, academic years ending 2003 & 2005.  
ECE Departmental Professor of the year 2002-2003  
Presented by Eta Kappa Nu student honor fraternity  
2002 NSF CAREER Award.  
1994 GLCTTR (Great Lakes Center for Truck & Transit Research) Scholar

## Professional Memberships & Service

Member of ACM  
Special Interest Group on Computer Architecture (SIGARCH)  
Special Interest Group on Simulation and Modeling (SIGSIM)  
Reviewer for PACT (Parallel Architectures and Compilation Techniques)  
Session Chair for SCOPES05 Conference

Member of IEEE  
IEEE Computer Society  
Advisor to Michigan Tech IEEE Computer Society student chapter  
Reviewer for IEEE Transactions for Embedded Systems  
Reviewer for MICRO-38 (IEEE/ACM International Symposium on  
Microarchitecture)

Member of ASEE

## Volunteer Activities

Served as a Judge in the Western U.P. Science Fair - sponsored by Omega Chi  
Epsilon. Each year in March 2002-2005  
Participated in and presented "Design and Construction of Computer Systems" to  
the Computer and Electrical Engineering MTU Summer youth programs  
Each Summer (July/August) for two or three weeks, 2002-2005.

## Selected Publications

### Refereed Journals

1. Vinodh Cuppu, Bruce Jacob, Brian Davis, Trevor Mudge. "High-Performance DRAMs in Workstation Environments." IEEE Transactions on Computers, November 2001. Volume 50, Number 11, pp. 1133-1153.

### Refereed Conference Publications & Proceedings

2. Jun Shao, Brian T. Davis, The Bit-reversal SDRAM Address Mapping, Proceedings of the 9th International Workshop on Software and Compilers for Embedded Systems (SCOPES05), Sept. 29, 2005 - Oct. 1, 2005. pp. 62-71.
3. Ying Zheng, Brian Davis, Matt Jordan. "Performance Evaluation of Exclusive Cache Hierarchies." International Symposium on Performance Analysis of Systems and Software, Austin Texas March 10-12, 2004. pp. 89-96.

4. Brian Davis, Trevor Mudge, Bruce Jacob, and Vinodh Cuppu. "DDR2 and Low-Latency Variants." Proceedings of the Solving the Memory Wall Workshop, held in conjunction with the 27th International Symposium on Computer Architecture (ISCA-2000). Vancouver BC, Canada, June 2000.
5. Vinodh Cuppu, Bruce Jacob, Brian T. Davis and Trevor Mudge, "A Performance Comparison of Contemporary DRAM Architectures", International Symposium on Computer Architecture, Atlanta Georgia, May 2-4 1999, pp.222-233.
6. Brian T. Davis, et.al., "Impact of MCM's on High Performance Processors", EEP-Vol. 19-1, Advances in Electronic Packaging - 1997 Conference, Volume 1, ASME 1997, pp.863-868.
7. Brian T. Davis and Trevor Mudge, "A Verilog Preprocessor for Representing Datapath Components", 4th International Verilog HDL Conference, March 1995, pp.90-98.

### **Invited publications**

8. B. Davis, T. Mudge, and B. Jacob. "The New DRAM Interfaces: SDRAM, RDRAM and Variants". In High Performance Computing, M. Valero, K. Joe, M. Kitsuregawa, and H. Tanaka, Editors, Vol. 1940 of Lecture Notes In Computer Science, Springer Publishing, Tokyo, Japan, 2000. pp. 26-31.

### **Reports**

9. Brian T. Davis and Paul Green, "Benefits of Sound for Driving Simulation: An Experimental Evaluation", University of Michigan Technical Report UMTRI-95-16, August 1995.

### **Papers Submitted, and in Review**

10. Divyakant.Gupta, Brian T.Davis and Kurt Pregitzer. "Web-Based Wireless Environment Sensing Network", Submitted to IEEE Transactions on Instrumentation & Measurement May 27, 2005.
11. Ying Xu, Jun Shao, Brian T. Davis, "Prediction in Dynamic DRAM Controller Policies", Submitted to the International Symposium on Computer Architecture, December 2, 2005.

### **Research Contracts**

Unisys, "Implementation of a DDR2 Controller using FPGA technology."

Brian T. Davis (PI), \$3300, 8/26/02 - 5/9/03

NSF Award, "REU: Research Experience for Undergraduates."

Brian T. Davis (PI), \$18,120, 7/01/02 - 6/30/07.

NSF Award # CCR-0133777, "CAREER: Memory Controller Interconnect and Policy Determination." Brian T. Davis (PI), \$442,385, 7/01/02 - 6/30/07.

Micron, "Hardware Implementation of a DRAM Controller."

Brian T. Davis (PI), \$5000, 8/01/01 - 4/30/02

## Graduate Students

### Ph.D Students

Jun Shao, expected graduation date June 2006

RongRong Lai, expected graduation date June 2009

### Masters Students

Gaurav Kulkarni, expected graduation date April 2007

Jing Zheng, expected graduation date December 2006

Ying Xu, expected graduation date April 2006

Srinivas Singampalli (M.S.E.E) “Multi Bus LAN simulation using Rational Unified Process”, defended 11/14/05

Divya Kant Gupta (M.S.E.E.) “Web-Based Wireless Environmental Monitoring System”, defended 4/26/05

David Pelster (M.S.E.E) “A Coursework Path Encompassing the Study of Computer Architecture within the Parallel Architecture Design Space.” defended 4/21/05, Placed with Intel, Folsom, CA.

Ali Pezeshk (M.S.E.E) “Design and Implementation of a 3D Computer Game Controller Using Inertial MEMS Sensors.” defended 12/07/04, Placed with Bosch, Farmington, MI.

Rade Trimceski (M.S.E.E) “Bluetooth Enabled Ad-Hoc Networks: Performance evaluation of a Self-Healing Scatternet Formation Protocol.” defended 8/23/04, Placed with Microsoft, Redmond, WA.

Shih-Ying Chou (M.S.E) “Embedded Linux Web Server” defended 12/10/03

Karttikeya Shah (M.S.E.E) “Design and Simulation of a Phased Locked Loop: Analog Circuit Design using Cadence.” defended 8/20/03, Placed with Maxim Electronics

Ying Zheng (M.S.E.E) “Exclusive Cache Architecture and Performance Evaluation.” defended 5/5/03, Placed with Intel, Shanghai.