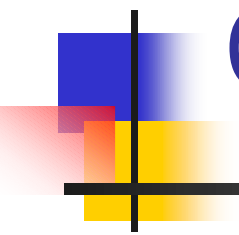
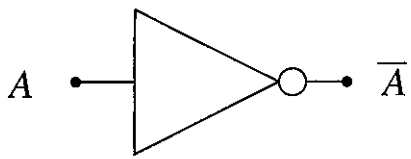
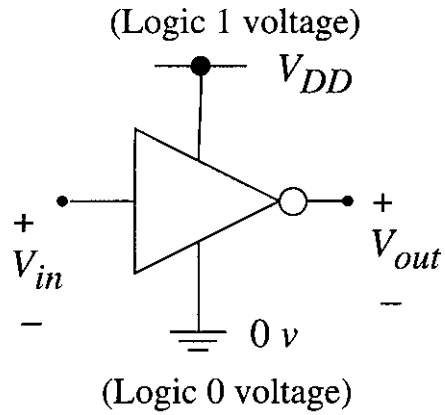


CMOS Circuits

An Inverter



(a) Logic symbol



(b) Electronic parameters

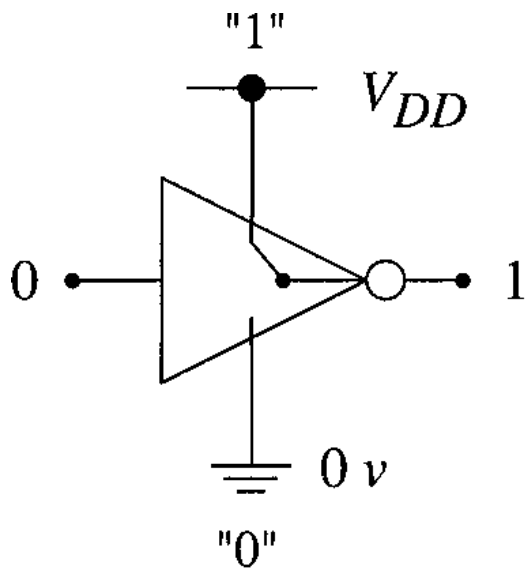
A	$\overline{A}$
0	1
1	0

(a) NOT truth table

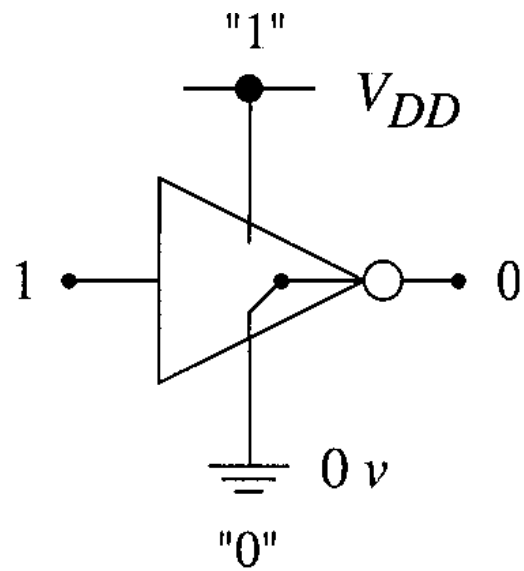
V_{in}	V_{out}
0v	V_{DD}
V_{DD}	0v

(b) Electronic equivalent

An Inverter

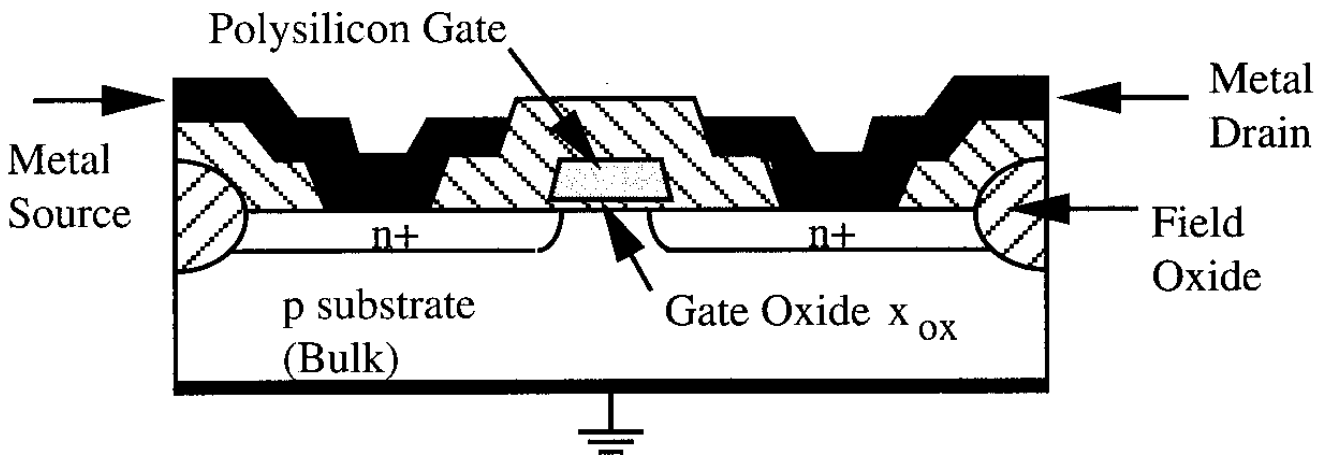


(a) Logic 0 input

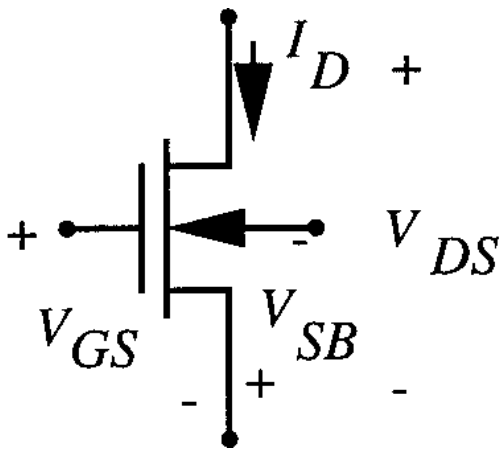


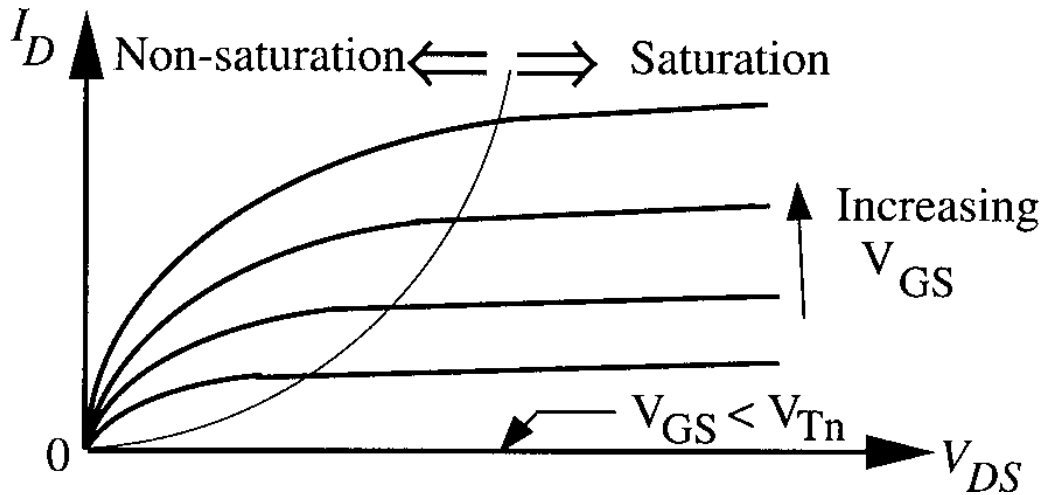
(b) Logic 1 input

Structure of an N-MOSFET

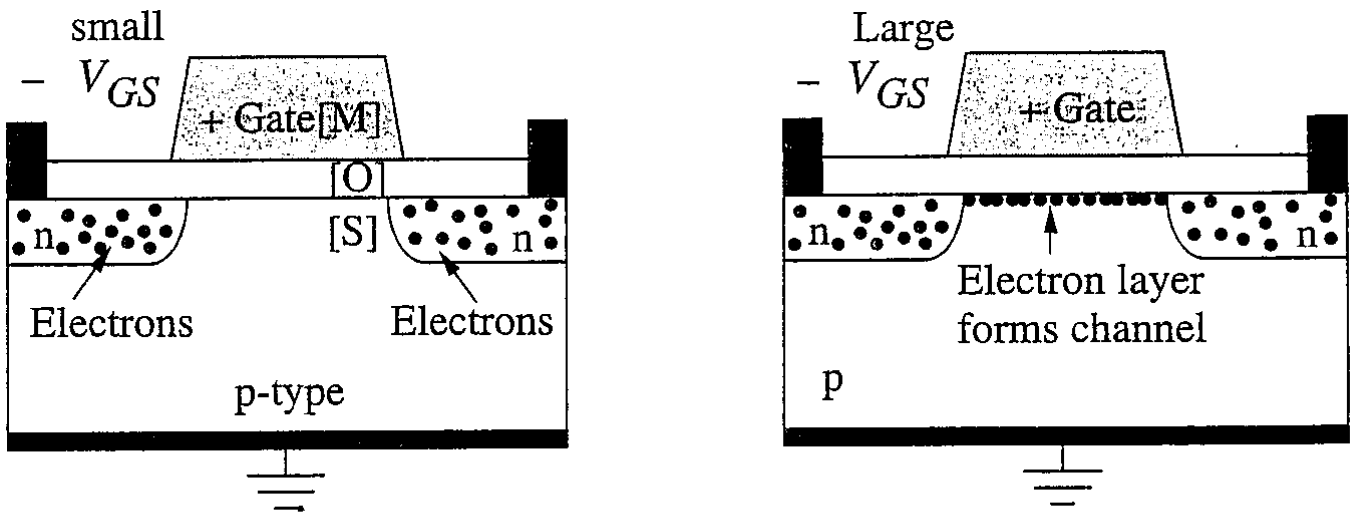


I-V Curve of n-MOSFET





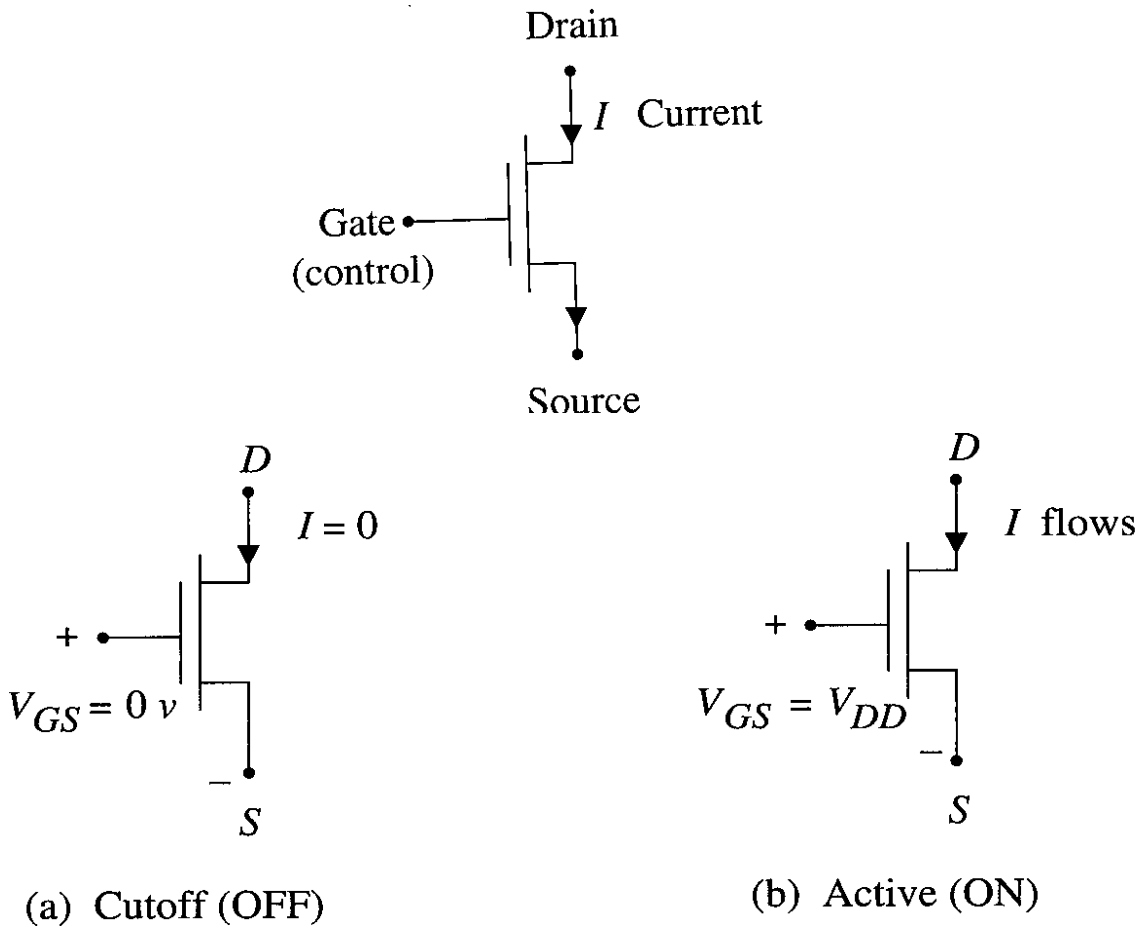
MOSFET Switching



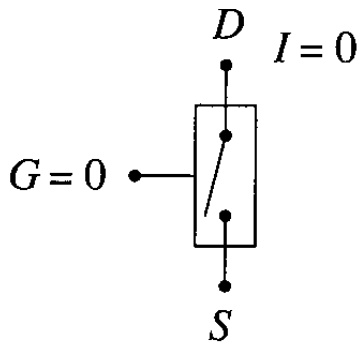
(a) Cutoff (open switch)

(b) Active (closed switch)

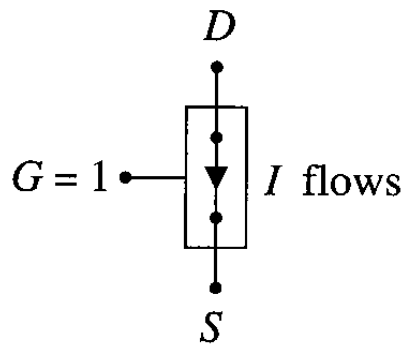
N-Channel MOSFET



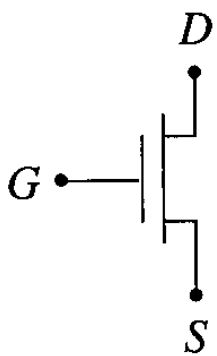
Switching Model of n-FET



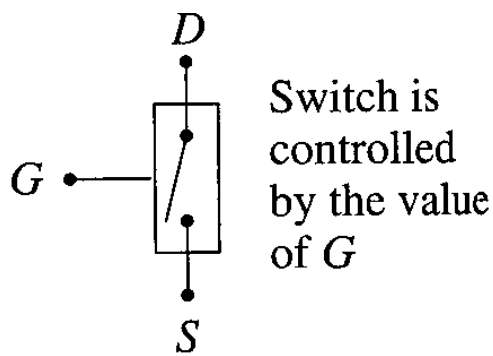
(a) OPEN switch



(b) CLOSED switch

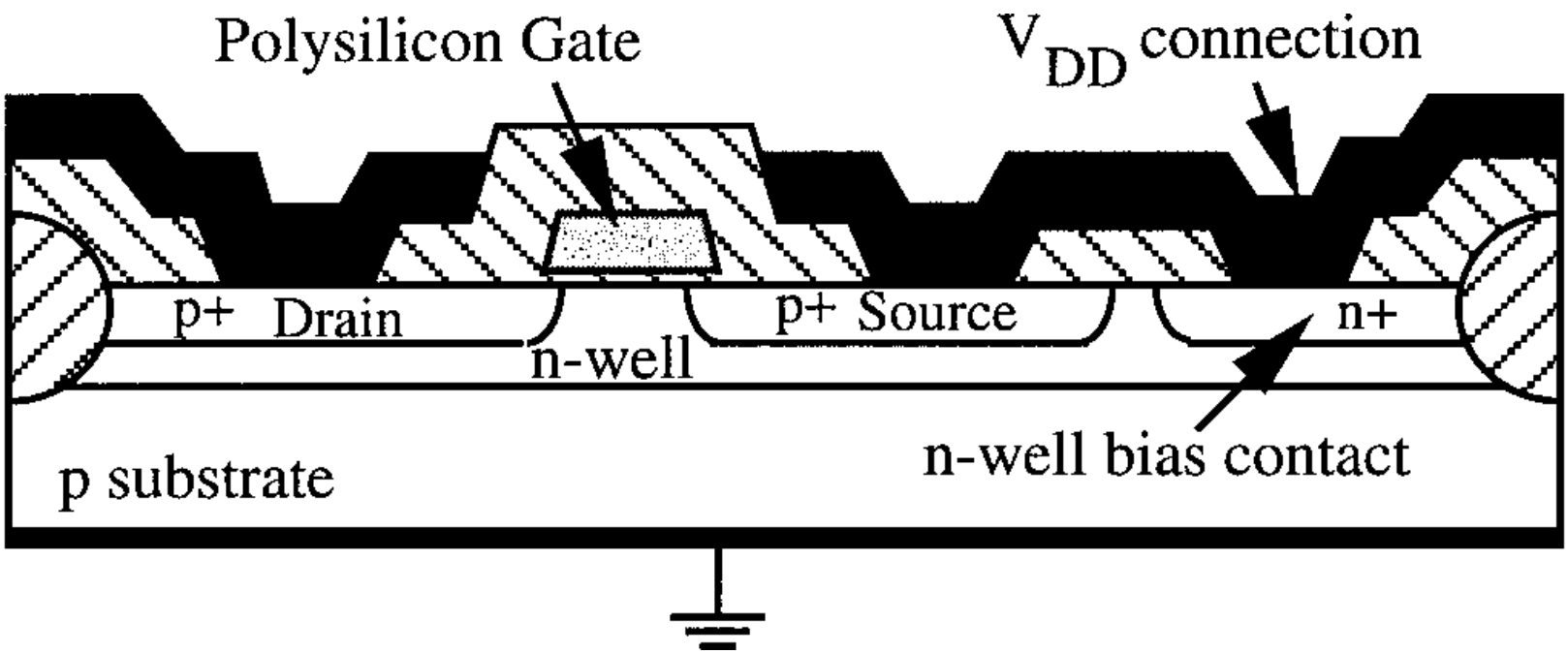


(a) Circuit symbol

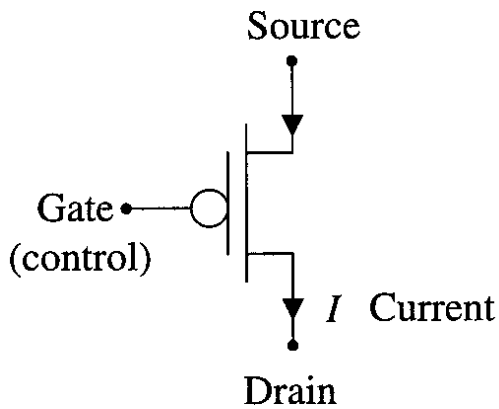


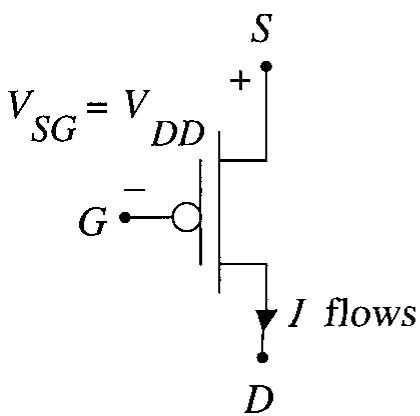
(b) Switch model

Structure of p-MOSFET

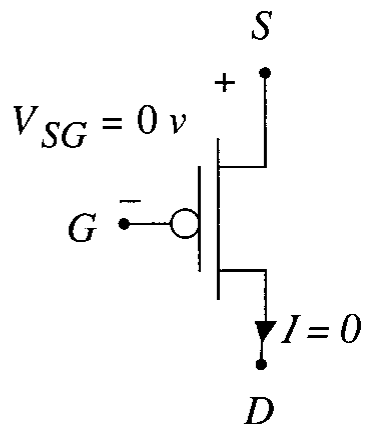


p-Channel MOSFET



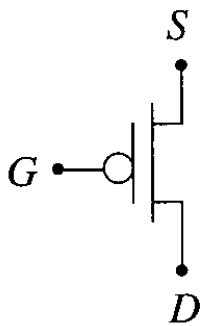


(a) Active (ON)

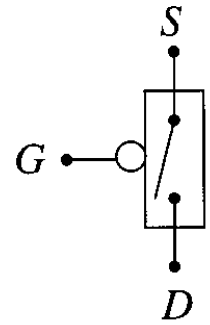


(b) Cutoff (OFF)

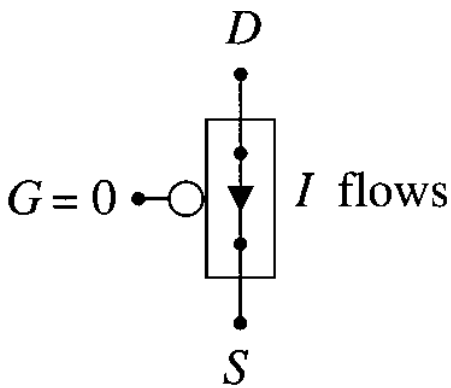
Switching Model of p-FET



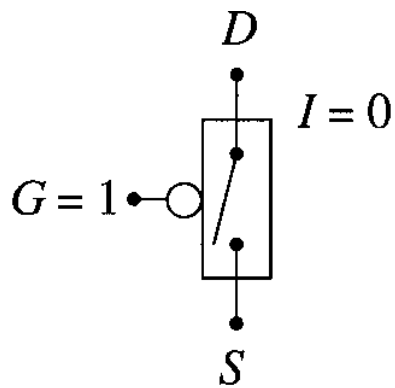
(a) Circuit symbol



(b) Switch model

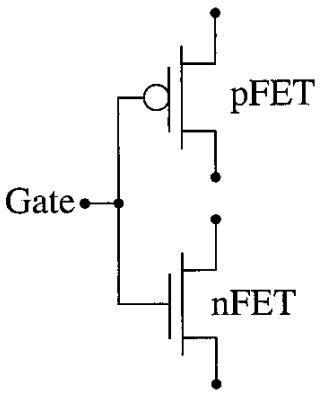


(a) CLOSED switch

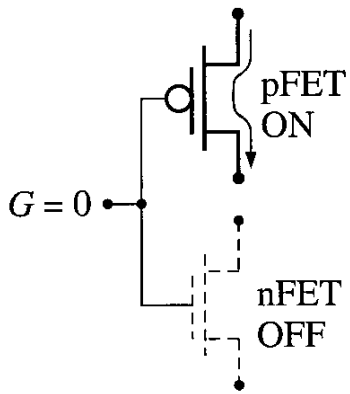


(b) OPEN switch

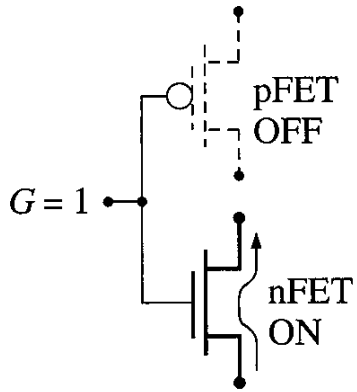
Complementary Pair of FETs



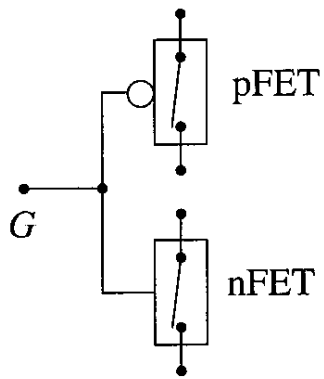
(a) nFET/pFET pair



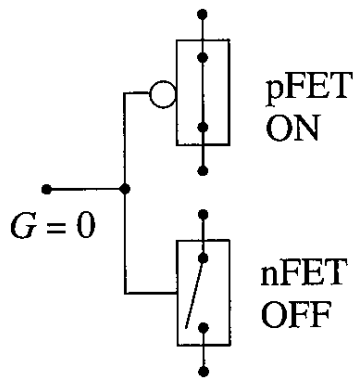
(b) Low gate voltage



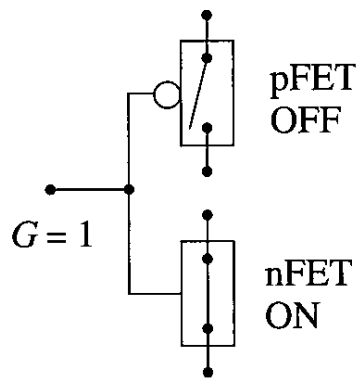
(c) High gate voltage



(a) nFET/pFET pair

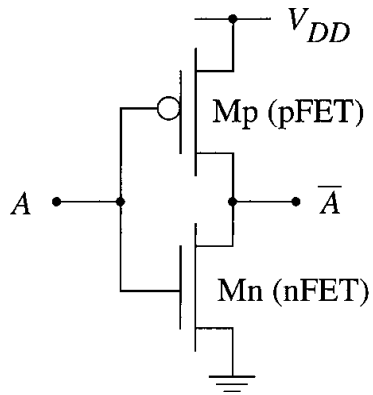


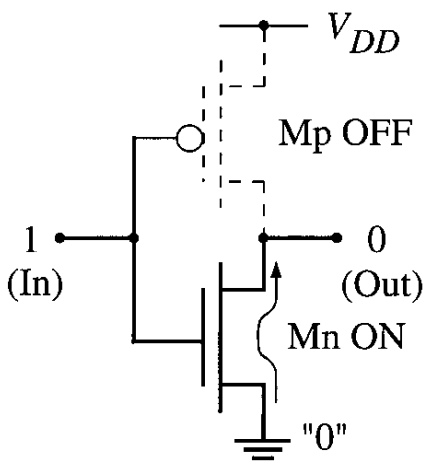
(b) $G = 0$ input



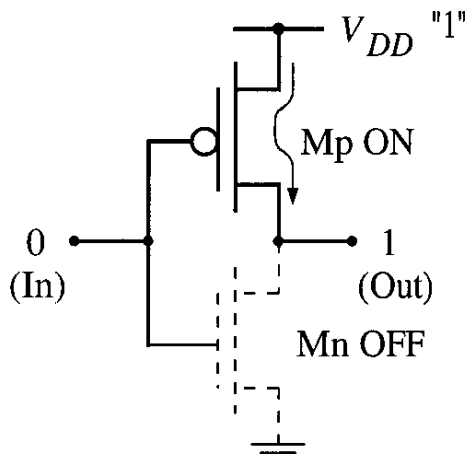
(c) $G = 1$ input

The CMOS Inverter



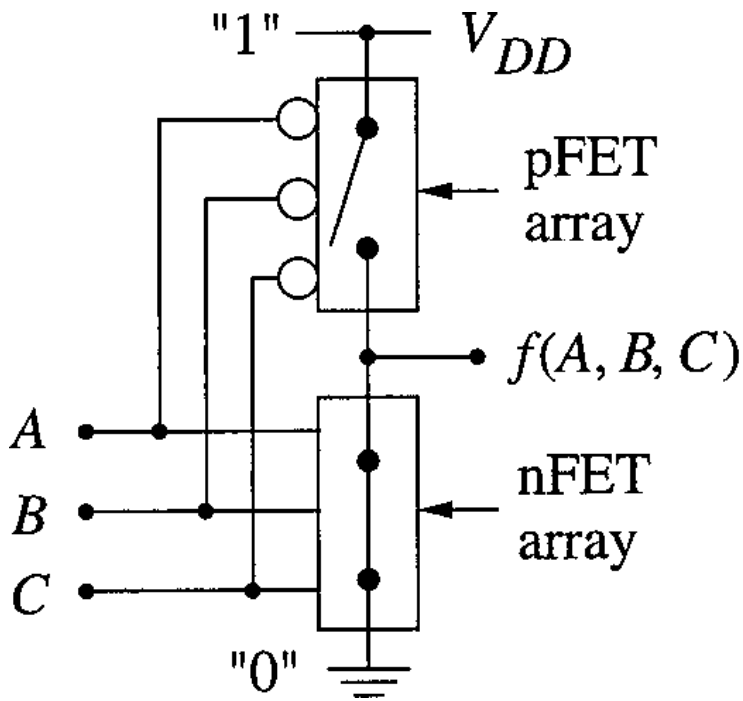


(a) Logic 1 input

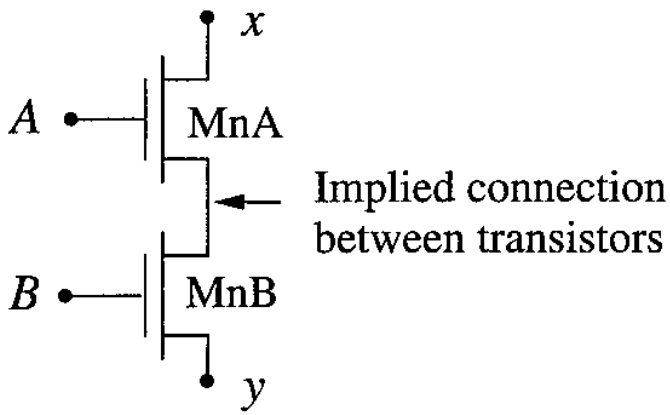


(b) Logic 0 input

3-Input CMOS Logic Gate

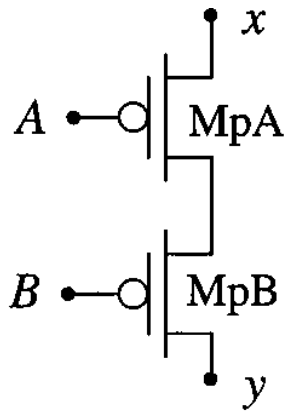


Series-Connected MOSFETs



x is connected to y
if and only if
$A = 1$ AND $B = 1$

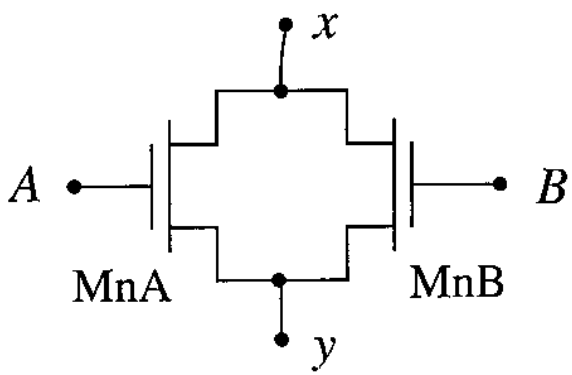
(a) nFET



x is connected to y
if and only if
$A = 0$ AND $B = 0$

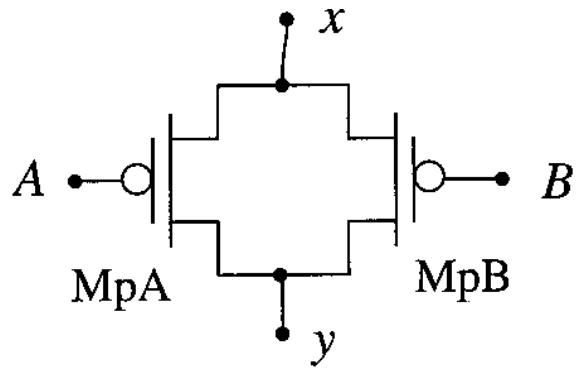
(b) pFET

Parallel-Connected MOSFETs



x is connected to y
if either $A = 1$ OR
$B = 1$ (or both)

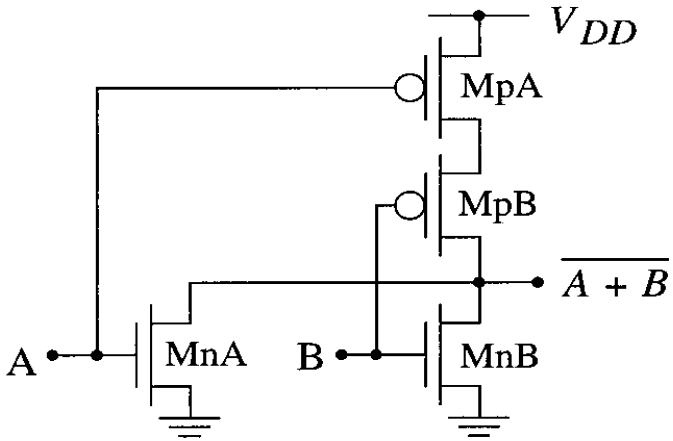
(a) nFETs



x is connected to y
if either $A = 0$ OR
$B = 0$ (or both)

(b) pFETs

CMOS NOR2 Gate

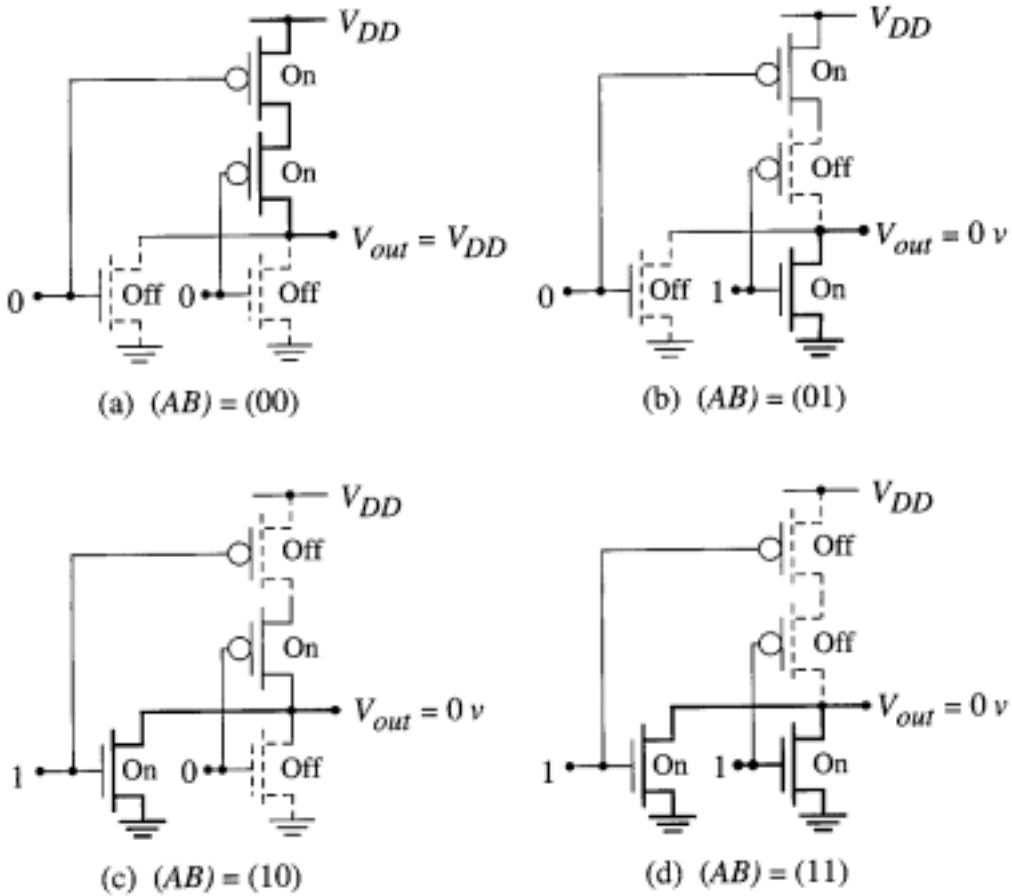


(a) CMOS circuit

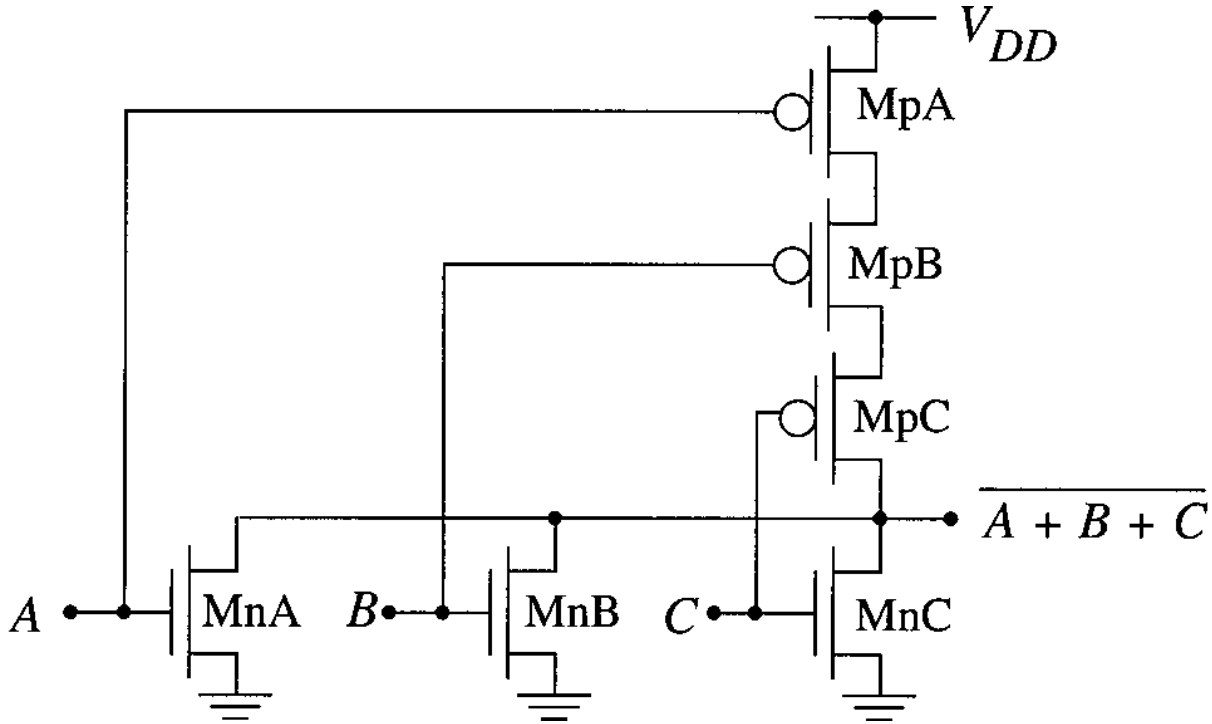
A	B	MnA	MnB	MpA	MpB	Out
0	0	OFF	OFF	**ON**	**ON**	1
0	**1**	OFF	**ON**	**ON**	OFF	**0**
1	0	**ON**	OFF	OFF	**ON**	**0**
1	**1**	**ON**	**ON**	OFF	OFF	**0**

(b) Operation summary

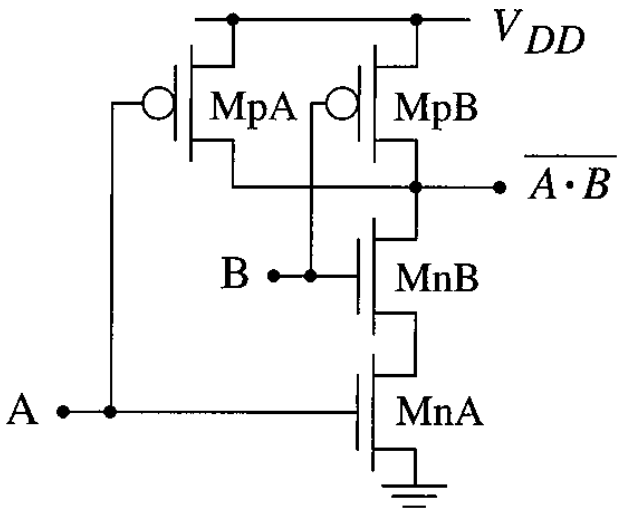
NOR2 Gate


V_{DD}
On
On
$V_{out} = V_{DD}$
0
Off
0
Off
(a) $(AB) = (00)$
V_{DD}
On
Off
$V_{out} = 0\ v$
0
Off
1
On
(b) $(AB) = (01)$
V_{DD}
Off
On
$V_{out} = 0\ v$
1
On
0
Off
(c) $(AB) = (10)$
V_{DD}
Off
Off
$V_{out} = 0\ v$
1
On
1
On
(d) $(AB) = (11)$

CMOS NOR3 Gate



CMOS NAND2 Gate

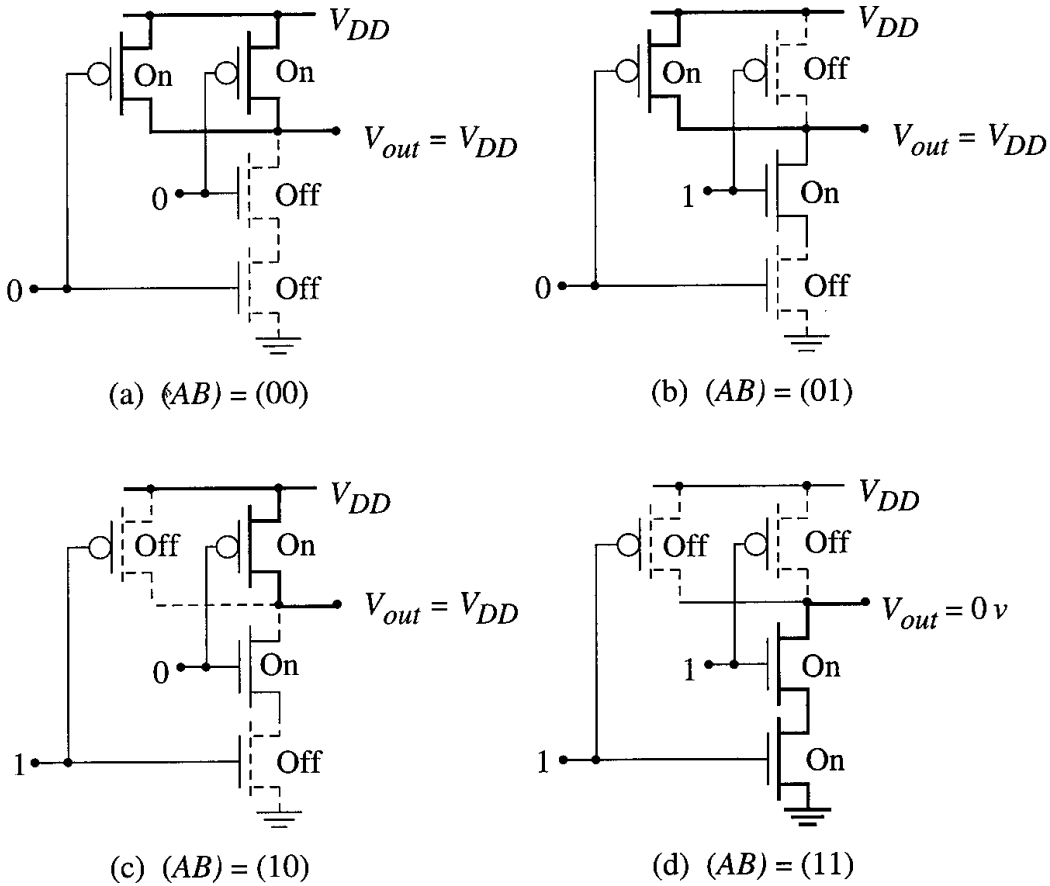


(a) CMOS circuit

A	B	MnA	MnB	MpA	MpB	Out
0	0	OFF	OFF	**ON**	**ON**	1
0	1	OFF	**ON**	**ON**	OFF	1
1	0	**ON**	OFF	OFF	ON	1
1	**1**	**ON**	**ON**	OFF	OFF	**0**

(b) Operation summary

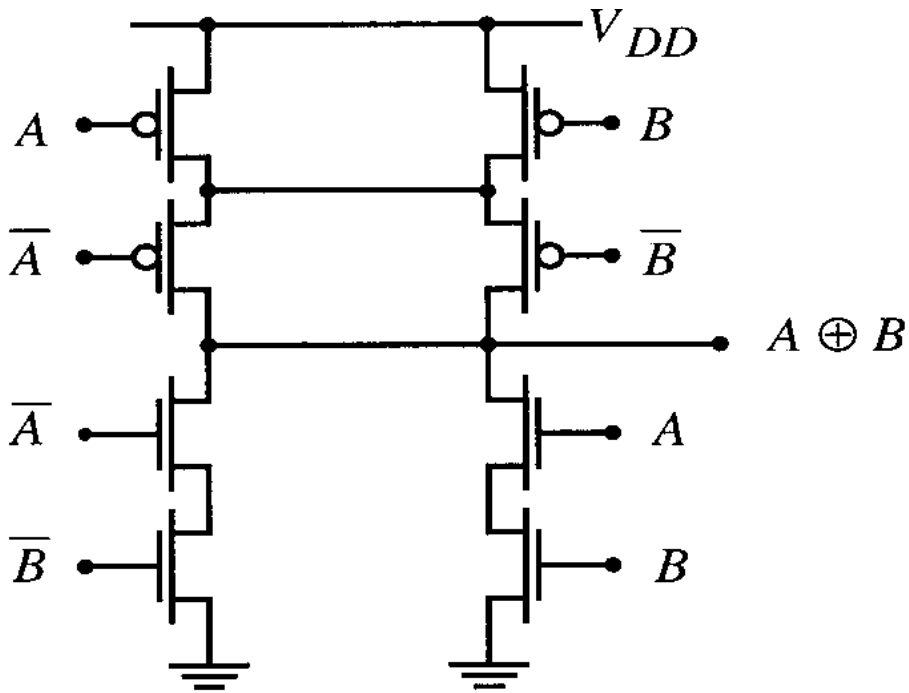
NAND2 Gate


V_{DD}
On
On
$V_{out} = V_{DD}$
0
Off
0
Off
(a) $(AB) = (00)$
V_{DD}
On
Off
$V_{out} = V_{DD}$
1
On
0
Off
(b) $(AB) = (01)$
V_{DD}
Off
On
$V_{out} = V_{DD}$
0
On
1
Off
(c) $(AB) = (10)$
V_{DD}
Off
Off
$V_{out} = 0\,v$
1
On
1
On
(d) $(AB) = (11)$

XOR Gate in CMOS

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

(a) Truth Table

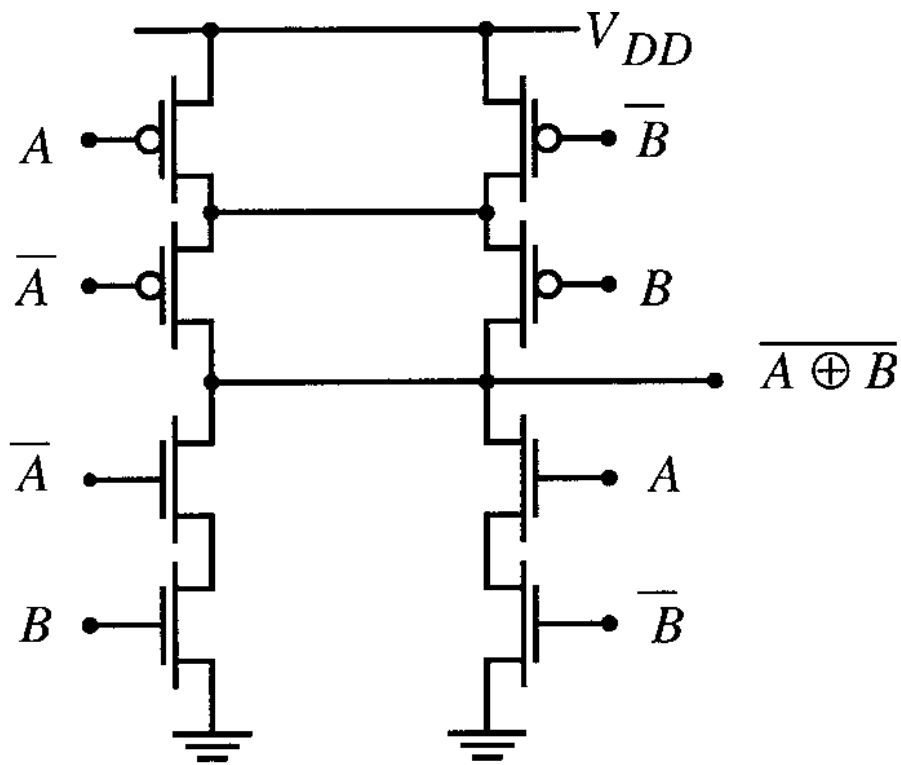


(b) Circuit

XNOR Gate in CMOS

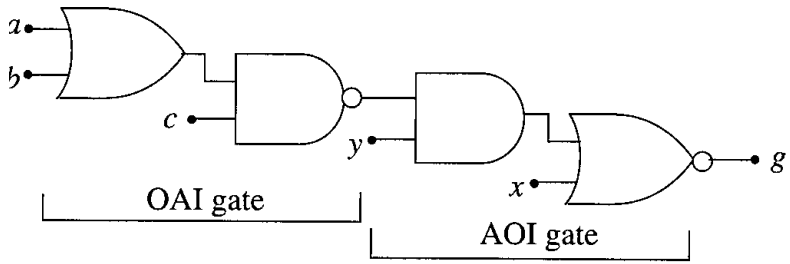
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

(a) Truth Table

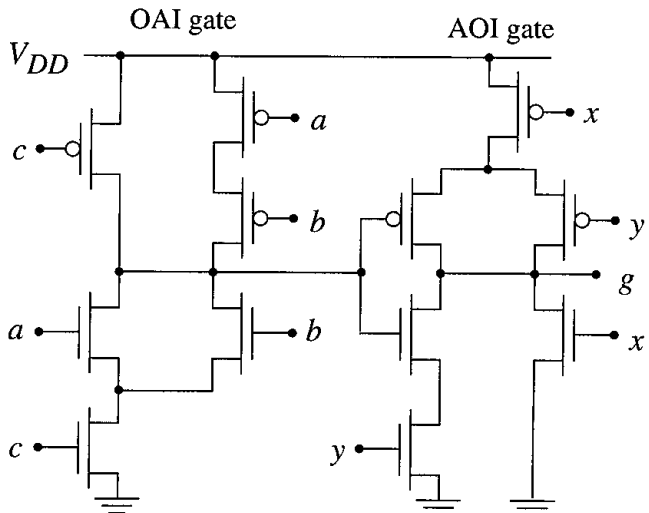


(b) Circuit

Logic Cascade in CMOS



(a) Logic diagram

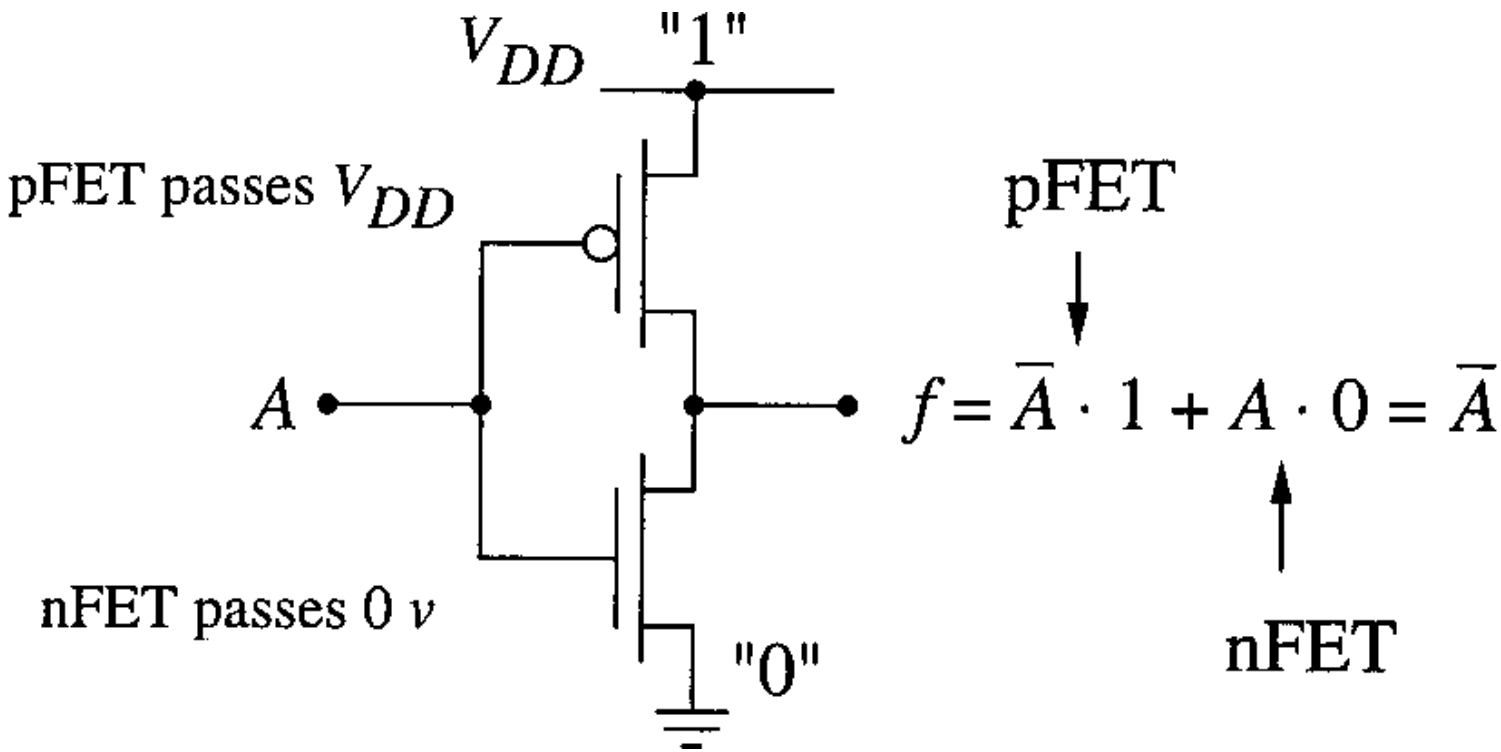


(b) CMOS cascade

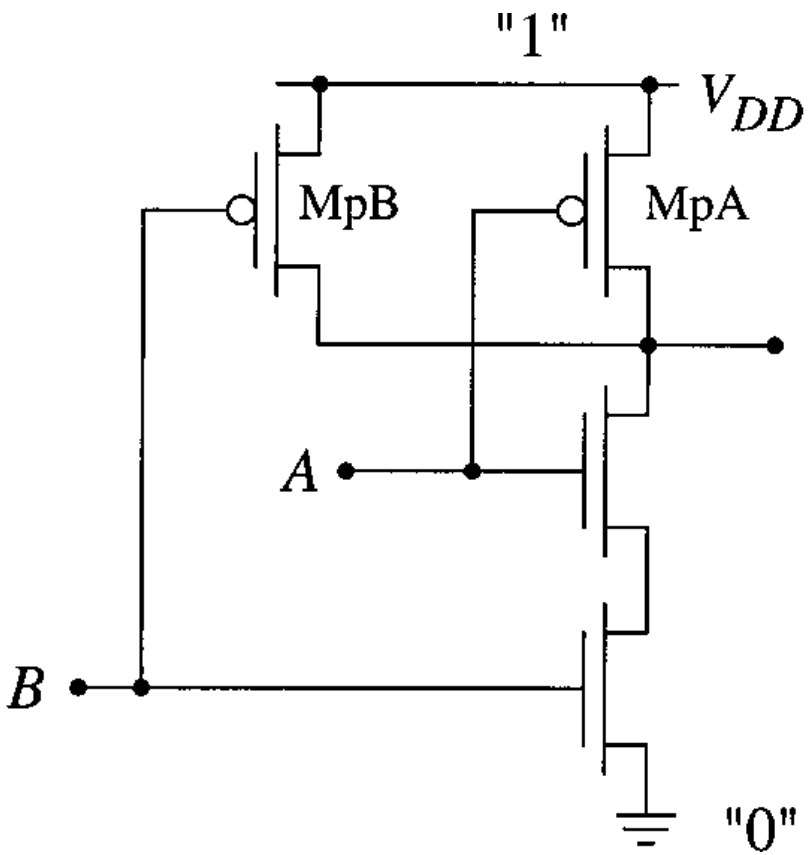
Logic Identities

OR Identities	AND Identities
$A + 0 = A$	$A \cdot 0 = 0$
$A + 1 = 1$	$A \cdot 1 = A$
$A + A = A$	$A \cdot A = A$
$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$
$\overline{\overline{A}} = A$	
$A + B = B + A$	$A \cdot B = B \cdot A$
$A + (B + C) = (A + B) + C$	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$
$A \cdot (B + C) = A \cdot B + A \cdot C$	$A + (B \cdot C) = (A + B) \cdot (A + C)$
$\overline{(A + B)} = \overline{A} \cdot \overline{B}$	$\overline{(A \cdot B)} = \overline{A} + \overline{B}$
$A + A \cdot B = A$	$A + \overline{A} \cdot B = A + B$

Logic Analysis – Inverter

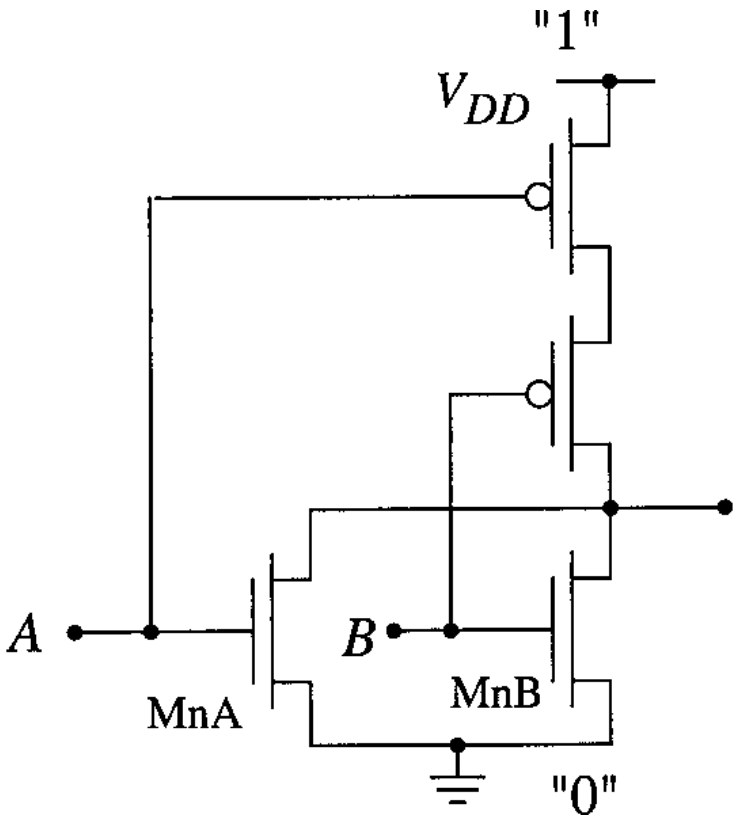


Logic Analysis – NAND Gate



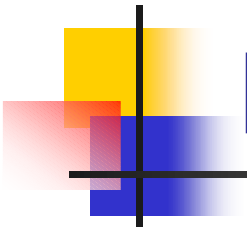
$$f = \underset{\text{MpA}}{\overline{A}} \cdot 1 + \underset{\text{MpB}}{\overline{B}} \cdot 1 + \underset{\text{nFETs}}{A \cdot B \cdot 0}$$
$$= \overline{A} + \overline{B}$$
$$= \overline{A \cdot B}$$

Logic Analysis – NOR2 Gate



MnA MnB pFETs

$$f = A \cdot 0 + B \cdot 0 + \overline{A} \cdot \overline{B} \cdot 1$$
$$= \overline{A} \cdot \overline{B}$$
$$= \overline{A + B}$$



References

- “Physical Design of CMOS Integrated Circuits” by J.P. Uyemura
- “Basic VLSI Design” by Pucknell and Eshraghian
- “Digital Systems Design” by J.P. Uyemura
- Other Books on VLSI Design