A New Twisted Differential Line Structure in Global Bus Design

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ABSTRACT

Twisted differential line structure can effectively reduce crosstalk noise on global bus, which foresees a wide applicability. However, measured performance based on fabricated circuits is much worse than simulated performance based on the layout. It is suspected that the via resistance variation is the cause.

In this paper, our extensive simulation confirm this. A new redundant via insertion technique is proposed to reduce via variation and signal distortion. In addition, a new buffer insertion technique is proposed to synchronize the transmitted signals, thus further improving the effectiveness of the twisted differential line.

Experimental results demonstrate that the new approaches are highly effective. Under a realistic setup, a 6GHz signal can be transmitted with high fidelity using the new approaches. In contrast, only a 100MHz signal can be reliably transmitted using a single-end model with power/ground shielding. In addition, compared to conventional twisted differential line structure, our new techniques can reduce the magnitude of noise by 45%. Furthermore, compared to unbuffered twisted differential line structure, the maximum signal phase difference is reduced from 37ps to 7ps by the new buffer insertion technique.

Categories and Subject Descriptors: B.8.2 [Performance and Reliability]:Performance Analysis and Design Aids

General Terms: Algorithm, Design, Performance, Reliability.

Keywords: Global bus, Differential line, Redundant via.

1. INTRODUCTION

With the VLSI technology scaling, global buses between function blocks become much longer and frequencies of signals become much higher. Subsequently, significantly more crosstalk are observed between neighboring bus lines, which causes the bus signal transmission unreliable.

Much research effort has been spent on reducing crosstalk and improving signal integrity on buses. Most of them focus on reducing capacitive crosstalk using single-end structure, for example, shielding and metal spacing [1]. They are capable of eliminating capacitive crosstalk since electrical field effect is of short range and tends to terminate in neighboring metal materials. In contrast, magnetic field effect is of long range, and thus these techniques can not suppress inductive crosstalk. As signal frequency increases, inductive crosstalk becomes as important as (i.e., comparable in magnitude to) capacitative crosstalk and is no longer negligible. Thus, it is imperative to consider both capacitive and inductive crosstalk in global bus design.

Differential signalling is such a technique. It is shown in [2] that 95.7% noise reduction can be obtained by this technique. However, [2] uses two parallel traces for each signal line, which can not effectively handle asymmetric noise sources. Thus, a twisted differential line structure (TDL) is proposed in [3], which differs from [2] in that the two traces can twist each other (through vias) periodically. This helps to balance the amount of noise at each trace. It is demonstrated in [4] that TDL can gain over 90% further noise reduction compared to untwisted differential structure. This foresees the wide applicability of TDL technique. However, measured performance based on fabricated circuits is much worse than simulated performance based on the layout. It is suspected that the via resistance variation is the cause. The problem aggravates with technology shrinking since both the nominal value and variation on via resistance are increasing. This imposes a great challenge in making twisted differential signalling technique practical.

In this paper, we first analyzed the reason that fabricated TDLs do not perform as expected. Through extensive simulation, we confirm that the cause of the performance degradation is via resistance variation. We then propose a new redundant via insertion technique to reduce the effect of via variation and signal distortion. In addition, we propose a new buffer insertion technique for signal synchronization.

Experimental results demonstrate a 6GHz signal can be transmitted with high fidelity using the new approaches. In contrast, only a 100MHz signal can be reliably transmitted using a single-end bus with power/ground shielding. Compared to conventional twisted differential line structure, our new techniques can reduce the magnitude of noise by 45% as witnessed in our simulation. Furthermore, compared to unbuffered twisted differential line structure, the maximum signal phase difference is reduced from 37ps to 7ps by the new buffer insertion technique.

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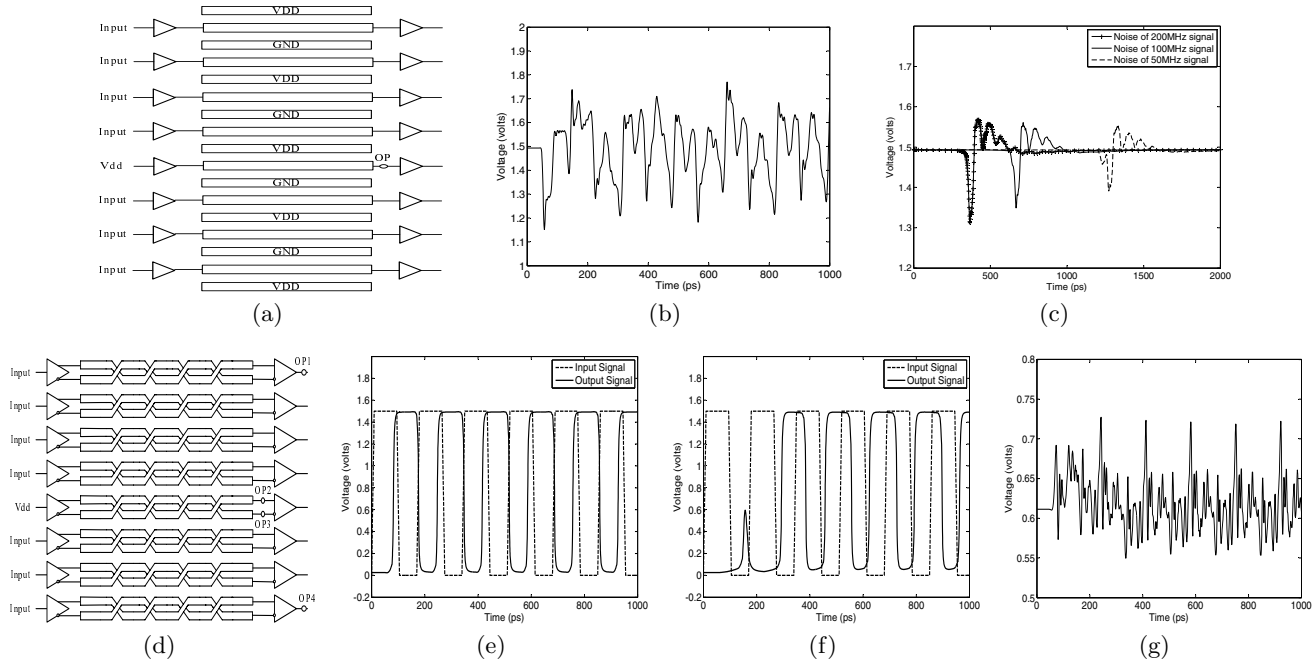

Figure 1: (a) A single-end model of 8-bit global bus. OP denotes the signal observation point. (b) Noise signal is measured at OP in Figure 1(a). The peak noise of 6GHz input signal is 0.35V. (c) The peak noise of 200MHz input signal is 0.18V, of 100MHz is 0.15V and of 50MHz is 0.11V. (d) A TDL structure of 8-bit global bus with single via. (e) Signal in TDL structure with single via and without variation. Output signal is measured at OP4 in Figure 1(d). (f) Signal in TDL structure with single via and with via variation. Output signal is measured at OP4 in Figure 1(d). (g) Noise signal in TDL structure with single via. Signal is measured at OP3 in Figure 1(d). The peak noise is 0.11V.

The rest of the paper is organized as follows. Section 2 describes single-end global bus structure and standard twisted differential line structure. Section 3 presents our new twisted differential line structure. A summary is given in Section 4.

2. EFFECT OF VIA VARIATION

2.1 Experiments Setup

The following realistic setup applies to all experiments. MOSIS 130nm technology [5] is used for our simulation. In an 8-bit global bus, each bit occupies an area of width of 2.5μm, height of 3μm, length of 3200μm, and space between adjacent bits is 2.5μm. Our aim is to design high speed bus, thus a 6GHz clock signal with a slew of 10ps is taken as the input signal. The power supply is 1.5V, and we define the acceptable noise margin is 10% of power supply as in [6], which is 0.15V. If signal exceeds the acceptable noise margin, we consider that a performance violation happens. The interconnect is modeled as 50 segments of unit length, and each segment uses the π model. FastHenry [7] is applied to extract both resistance and inductance. An accurate empirical model [8] is applied to extract capacitance of interconnects. SPICE is used for the simulation.

2.2 Single-end Bus Structure

We perform simulation on the widely used single-end bus structure with power/ground shielding. The schematic is shown in Figure 1(a). In this structure, each signal line is sandwiched by a power trace and a ground trace, which can almost fully protect the signal line from capacitive crosstalk. Each signal line is also provided with an adjacent current return path, which could help reduce the inductive crosstalk. To test the worst-case noise generated on the 8-bit bus, a 6GHz signal is sent to all the inputs except the one in the middle. The middle line, called *observation line*, serves as the observation point for the noise. Buffers are used as drivers and receivers. SPICE simulation result is shown in Figure 1(b). One sees that the peak noise is 0.35V, which exceeds the acceptable noise margin.

Since the desired 6GHz signal cannot be transmitted reliably, we investigate the highest signal frequency which can be achieved using single-end bus. In the power/ground shielding bus model, the noise will not fall into the acceptable margin unless we decrease the input signal frequency (signal slew is fixed as 10% of signal period) to 100MHz. Refer to Figure 1(c). It is clear that the conventional single-end bus model is not sufficient to handle high frequency signal transmission even if power/ground shielding technique is incorporated.

2.3 Standard Twisted Differential Line Structure

In the twisted differential line structure (TDL) in Figure 1(d), for each bit line, two parallel traces are used to transmit the complementary signals and the two traces are twisted periodically. At a twisting point, one trace keeps its route while the other goes down and then up across metal layers. Two vias are needed for each twisting. The twisted differential line structure is very effective in noise reduction since each trace receives balanced noise from the environment, regardless of the location of noise source.

However, the transmitted signals after fabrication suffer huge distortion even if the signals function correctly in layout simulation. It is suspected that via resistance variation is the cause. In order to justify our statement, we perform

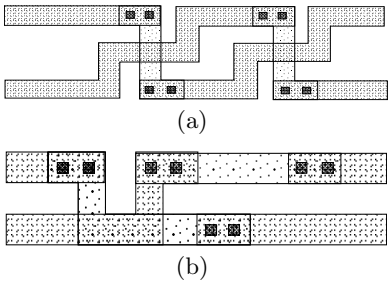

Figure 2: Two layouts of TDL structure with double vias using Virtuoso. Both designs are symmetric for delay balance and noise reduction.

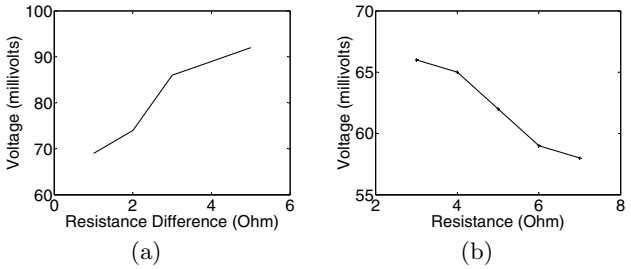

Figure 3: Peak noise is measured at OP3 in Figure 1(d). (a) The peak noise with respect to the resistance difference between two neighboring traces. (b) The peak noise with respect to the resistance in two neighboring traces. The resistance of two neighboring traces is the same.

intensive simulation considering different sources of variation, e.g. gate length, gate oxide thickness, interconnect height and via resistance.

As a realistic setup, each trace of bus has 4 twisting points, that is, 8 vias in total for each two complementary traces. The nominal value of the via resistance is 5Ω, and it varies from 3Ω to 7Ω [9]. The nominal value of gate length, gate oxide thickness and interconnect height is from MOSIS 130nm technology [5]. From our simulation result in Figure 1(e), one sees that without any variation, the input signal can be transmitted in high quality.

A relationship between via resistance variation and other variation is established in the simulation. With 10% via resistance variation, the impact to the output signal is equal to 30% gate length variation, 20% gate oxide thickness variation or 15% interconnect height variation. This demonstrates that the via resistance variation has a larger impact on the output signal. When worst-case via variation is considered, the logic failure of output signal happens. From Figure 1(f), one can see that the input signal originally is 101010101010, however, the output signal turns into 001010101010. These simulations demonstrate that via variation have critical impact on signal transmission on global bus and via resistance increases with technology shrinking. As it turns out, the vias are bottlenecks of performance of TDL.

This imposes a great challenge on high-speed bus design. Note that although signal can not be reliably transmitted when via variation are considered, the noise is still significantly reduced. The noise is shown in Figure 1(g). The peak noise is 0.11V, compared with 0.35V in the single-end structure shown in Figure 1(b).

3. NEW TWISTED DIFFERENTIAL LINE STRUCTURE

Based on a redundant via insertion technique and a buffer insertion technique, a new twisted differential line structure is proposed. With it, the hurdle of signal distortions associated with the standard TDL is overcome. This makes the TDL technique, which is very effective in reducing both capacitive and inductive noise, practical in high speed global bus design. We envision the new TDL structure to have wide applicability in practice.

We begin with investigating the relationship between crosstalk noise and redundant via. The effect of redundant via is twofold: First, redundant via reduces the resistance variation/difference between neighboring traces. Second, redundant via reduces the nominal resistance value of neighboring traces. Figure 3(a) shows that peak noise increases with the resistance difference between neighboring traces. Figure 3(b) shows that peak noise decreases with resistance of neighboring traces. The two figures demonstrate that the twofold effect of redundant via competes each other, and since the peak noise is more sensitive to the resistance difference, the crosstalk noise can be reduced by redundant via insertion technique. This observation will be explored in the following section.

3.1 Redundant Via Insertion

TDL needs vias to connect between neighboring metal layers. With technology scaling, via size keeps shrinking and via contact resistance keeps increasing. The problem aggravates since variation on via due to cut misalignment, electro migration and thermal stress increases. As a consequence, distortions in signal transmission are observed.

To tackle this issue, we propose to insert redundant vias into the initial design. Given a via (which is around a twisting point in TDL), putting $n-1$ additional vias in its close proximity can reduce the nominal value of the resistance to $1/n$ and variation of the conductance to $O(1/n^2)$. In addition, doing so will also reduce the effect of variation on vias. On the other hand, one might wonder the effect of the additional cost (e.g., power) due to the inserted redundant vias. Since a global bus often has very few twistings/vias, doubling/tripling them will not cause trouble. In fact, redundant via methodology has been recommended as an effective technique to improve yield by major foundries in their $130nm$ and $90nm$ processes [10]. Major EDA vendors such as Cadence and Synopsis have already allowed the feature of redundant via insertion in bus routing design [11] without violating any design rule. Figure 2 shows two different layouts using Virtuoso.

As shown in Figure 1(f), standard TDL with single via fails to transmit high frequency signal. We apply our redundant via insertion technique in the same simulation environment. Figure 4(a) shows the output signal after adding another via, which well matches the input signal.

The crosstalk noise is also reduced by redundant via technique. Figure 4(b) shows the crosstalk noise in TDL with double vias. The peak noise is 0.08V, compared with 0.11V of standard TDL with single via in Figure 1(g).

The comparison of TDL performance between single via and double vias is summarized in Table 1. Suc. represents

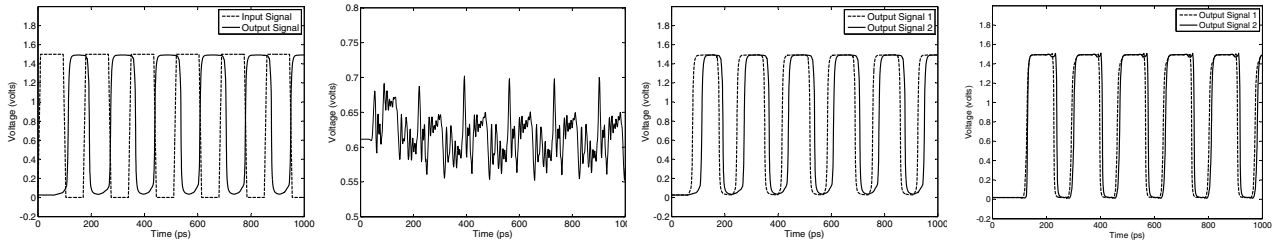

Figure 4: (a) Input signal and output signal in TDL structure with double vias. Output signal is measured at OP4 in Figure 1(d). (b) Noise signal in TDL structure with double vias. Signal is measured at OP3 in Figure 1(d). The peak noise is 0.08V. (c) Output signals in twisted differential line structure with double vias. Output signals are measured at OP1 and OP4 in Figure 1(d). The maximum output difference is 37ps. (d) The maximum output difference is 7ps.

that the noise falls in the acceptable margin and output signal has no logic failure. When input frequency is higher than 5GHz, TDL with single via has logic failure in the output. In the contrast, TDL with double via reliably transmits input signal to the output. In the meantime, the noise and output delay difference of double via circuit is consistently less than these of single via circuit.

Table 1: Comparison of TDL performance between single via and double vias. D.D. denotes maximum delay difference.

Test Freq.	Single Via			Double Vias		
	Noise (volt)	D.D. (ps)	Suc.	Noise (volt)	D.D. (ps)	Suc.
100MHz	0.02	29	YES	0.02	21	YES
500MHz	0.03	42	YES	0.02	21	YES
1GHz	0.04	42	YES	0.03	24	YES
2GHz	0.05	43	YES	0.03	34	YES
3GHz	0.06	44	YES	0.04	34	YES
4GHz	0.06	45	YES	0.05	35	YES
5GHz	0.09	-	NO	0.06	35	YES
6GHz	0.11	-	NO	0.08	37	YES

3.2 Buffer Insertion

The output signals can be out of synchronization in global bus due to via resistance difference and delay difference on each trace, which is often observed in our simulation. An example is shown in Figure 4(c), where the delay difference between the two output signals is 37ps, which is almost 1/4 of signal period. There are previous works on applying buffer insertion to global bus design [12]. However, all of them focus only on noise reduction, since in previous bus design, signal traces are either singled-ended or not twisted. In the new TDL design, buffer insertion is applied to handle signal synchronization.

Denote by *sync-error* the maximum delay difference between signal traces at the receiver. Thus, we are to reduce sync-error in a bus design by buffer insertion.

Details of algorithm are omitted due to space limit. A highly effective pruning technique and a buffering pattern based timing evaluation method are proposed in the algorithm.

The simulation result after buffer insertion is shown in Figure 4(d). The sync-error decreases to 7ps compared with 37ps in Figure 4(c). As a comparison, we perform some buffer insertions by hand and the results are consistently worse compared to the above result. The sync-error of our best result by hand is 12ps. Along with sync-error, crosstalk noise can be further reduced by buffer insertion. The peak noise is 0.06V, which is 45% of 0.11V in standard TDL with single via.

4. CONCLUSION

Although twisted differential line (TDL) design is highly effective for noise reduction, its applicability is greatly compromised due to large signal distortion resulting from high via resistance. This challenge is tackled in this paper. A redundant via insertion technique is proposed to reduce signal distortions. In addition, a buffer insertion technique is proposed to handle signal synchronization in TDL design. Our experimental results demonstrate that under a realistic setup, a 6GHz signal can be transmitted with high fidelity using our new approaches. In contrast, only a 100MHz signal can be reliably transmitted using a single-end bus structure.

5. ACKNOWLEDGEMENTS

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