Buffering Single-Walled Carbon Nanotubes Bundle Interconnects for Timing Optimization

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***Abstract*— As prevailing copper interconnect technology advances to its fundamental physical limit, interconnect delay due to ever-increasing wire resistivity has greatly limited the circuit miniaturization. Single-walled carbon nanotubes (SWCNTs) bundle interconnects have emerged as a promising replacement material for copper interconnects due to their superior conductivity. Previous works have focused on studying device and interconnect modeling for bundled SWCNTs while none of them consider deployment of such an advanced technology into VLSI physical design.**

To the best of the authors' knowledge, this paper develops the first physical design technique for the interconnect optimization using carbon nanotube interconnects. We propose a timing driven buffer insertion technique for bundled SWCNTs, where the standard buffering algorithm has been enhanced to accommodate some features in the SWCNT timing modelling. Our experimental results on a set of scaled industrial nets at 22nm technology demonstrate that compared to copper buffering, CNT buffering can save over 50% buffer area with the same timing constraint. In addition, CNT buffering can effectively reduce the delay by up to 32%. Further, CNT buffering runs in time similar to copper buffering.

***Index Terms*–** Carbon Nanotube, Bundled SWCNTs, Interconnect Optimization, Buffer Insertion, Timing Optimization.

I. Introduction

As one of the most effective interconnect timing optimization techniques, copper buffer insertion is indispensable in physical design [1], [2], [3], [4], [5]. However, since copper interconnect technology has its fundamental physical limit, interconnect delay due to ever increasing wire resistivity has greatly limited the circuit miniaturization. The electromigration induced interconnect reliability issue resulting from the inherently low tolerable current density in copper interconnect aggravates the problem. Consequently, the novel on-chip interconnect material is highly desirable as a replacement of copper interconnect in nanoscale high-speed circuit design. As promising replacement materials, carbon nanotubes (CNTs) alleviate the above severe timing and reliability issues in copper interconnect due to their superior conductivity and current carrying capabilities. CNTs have significantly larger carrier mean free paths and can conduct larger currents without deterioration compared to copper interconnects [6]. As a result, the issues such as electromigration that plaque the copper interconnects are mitigated. In addition, CNTs have high thermal conductivity and mechanical stability.

CNTs are miniaturized tubes consisting of rolled up sheets of carbon hexagons. There are two main types of CNTs with structural perfection. Single-walled carbon nanotubes (SWCNTs) are composed of a single graphite sheet seamlessly wrapped into a cylindrical tube while multi-walled carbon nanotubes (MWCNTs) are composed of an array of concentrically nested CNTs. Since a single CNT has much larger resistance than copper for global interconnect [7], it is desired to bundle CNTs in parallel, resulting in *bundled CNTs*, for better performance. According to [7], it is difficult to use MWCNTs for long-length ballistic transport, thus, this paper will focus on the popular bundled SWCNTs. Various research efforts have been spent in CNT fabrication. Most of them explores chemical vapor deposition technologies and successful fabrication experience on CNT includes [8], [9], [10], [11], [12], [13].

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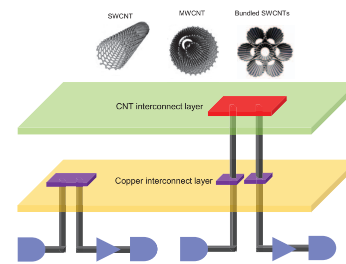

Fig. 1. Copper buffering and CNT buffering.

It has been shown that bundled SWCNTs can outperform copper interconnects in signal wave transportation along a long global interconnect [7], [14], [15], [16], [17]. For example, it is shown in [7] that the resistance of bundled SWCNTs can be achieved 50% smaller compared to that of copper at the same size of a long interconnect at $22nm$ technology node. Despite this, buffer insertion is still necessary to improve the timing of a bundled SWCNTS. Although there are works [7], [14] which consider CNT interconnect, they always use a two pin model since their perspective is from the device and interconnect modeling of CNTs. None of existing works consider the deployment of such an advanced technology into the VLSI physical design. To the best of the authors' knowledge, this paper presents the first physical design technique considering carbon nanotube interconnects. Refer to Figure 1. The CNTs are replacing copper in global interconnect. In this paper, bundled SWCNTs are mainly considered. The main contribution of this work is summarized as follows.

- The timing driven buffer insertion technique for bundled SWCNTs is proposed which can handle signal net buffering in VLSI design. To the best of authors' knowledge,

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this is the first buffer insertion optimization for CNT interconnects in the literature.

- Timing driven buffering algorithm for copper interconnect has been adapted to handle bundled SWCNTs.
- Our experiments are conducted with 500 scaled industrial nets and 10 different types of scaled buffers and inverters at 22nm technology. With the same timing constraint, CNT buffering can save over 50% buffer area compared to copper buffering. In addition, it is demonstrated that CNT buffering can effectively reduce the delay by up to 32%.

II. Problem Formulation

Consider a routing tree $T = (V, E)$ where $V = s_0 \cup V_s \cup V_n$, and $E \in V \times V$. Let $|V| = n$. Vertex s_0 is the source node and also called the root of the tree. V_s is the set of sink nodes. Each sink, denoted by s, has a sink capacitance and required arrival time $RAT(s)$. T is said to satisfy the timing constraint if its required arrival time at root is no earlier than the arrival time at root. Each edge, denoted by e, in E represents a segment of wire, which has edge resistance $R(e)$, edge inductance $L(e)$ and edge capacitance $C(e)$. V_n refers to the candidate buffer positions where the buffers can be inserted. In practice, they are discrete locations and are specified before buffer insertion algorithm by e.g., wire segmenting technique [18].

A buffer library B which consists of a set of different types of buffers are given to the buffering problem. Let $|B| = m$. Each buffer, denoted by b, has its cost $W(b)$, input capacitance $C(b)$, driving resistance $R(b)$ and intrinsic delay $t(b)$. Following most existing buffering works [1], [2], [3], [4], [5], the underlying routing tree can be assumed to be binary since trees in other topologies can be converted to a binary one using the technique in [3]. Given a tree in carbon nanotube interconnect layer, a buffer assignment is to determine the locations and the types of buffers which will be inserted to the routing tree. Our buffer insertion problem is formulated as follows.

Timing Constrained Minimum Cost Buffering for Carbon Nanotube Interconnects: Given a binary routing tree with n candidate buffer locations in carbon nanotube interconnect layer, a buffer library and a set of candidate buffer positions, to compute a buffer assignment solution such that the timing constraint is satisfied, and the total buffer cost is minimized.

III. Carbon Nanotube Interconnects

To tackle the fundamental physical limits on copper interconnects, CNTs have emerged as a promising replacements for Copper interconnects due to their better conductivity and current carrying capabilities. Table I from [19], [20] summarizes some major advantages of CNTs over copper interconnects. In fact, similar observations have been made from many other works [21], [22], [23], [24], [25].

TABLE I
Comparison between CNT and copper interconnect [19], [20].

Properties	CNT	Cu
Max. current density	$10^{10} A/cm^2$	$10^6 A/cm^2$
Mean free path	$1000nm$	$40nm$
Thermal conductivity	$6000\ W/mK$	$400\ W/mK$

CNTs are miniaturized tubes consisting of rolled up sheets of carbon hexagons. Figure 2 shows an equivalent circuit model for an isolated single-walled carbon nanotube (SWCNT), which is proposed in [7]. It has become a popular model and it will be explained how to compute the resistance and capacitance using this model.

A. Resistance for CNT

1) Resistance for An Isolated SWCNT: The resistance of an isolated SWCNT, denoted by $R_{isolated}$, is divided into two parts, the quantum resistance R_Q and scattering resistance R_S as shown in Figure 2. Recall that the mean free path, denoted by λ, refers to the average distance between two subsequent collisions of electrons. The mean free path of electrons for a CNT is about $1\mu m$ as shown in Table I, i.e., $\lambda = 1\mu m$. When $l \le \lambda$ where l is the length of a carbon nanotube, we have [26]

$$R_Q = \frac{h}{4e^2} = 6.45k\Omega, \tag{1}$$

where e is the electronic charge and h is Plank's constant. Thus, if the length l of a CNT is less than $\lambda = 1\mu m$, the resistance of CNT is independent of length.

For the length greater than the mean free path, the distributed scattering resistance for an interconnect with length l is [26], [27]:

$$R_S l = \frac{hl}{4e^2\lambda}. \tag{2}$$

For simplicity, one defines $R_S = 0$ when $l \le \lambda$. In practice, the total resistance of a single CNT, denoted by $R_{isolated}$, is expressed as the sum of quantum resistance and scattering resistance as shown in the following equation [7]

$$R_{isolated} = R_Q + R_S l. \tag{3}$$

Comparing to copper global interconnect, a single SWCNT global interconnect has resistance of $6.45k\Omega/\mu m$, which is too large for timing minimization. However, if a bundled SWCNTs are used, the resistance can be significantly reduced.

2) Resistance for a Bundled SWCNTs: The resistance of a bundle, denoted by R_{bundle}, is given by the following equation [27]:

$$R_{bundle} = R_{isolated}/N_{cnt}, \tag{4}$$

where N_{cnt} is the number of CNTs contained in the bundle. It is clear that the resistance decreases with increasing N_{cnt}.

3) Contact Resistance: Due to the presence of imperfect metal and carbon nanotube contacts, contact resistance needs to be considered. According to [17], some research groups have accomplished to fabricate the contact resistances ranging from a few hundred ohms to a few kilohms which have similar magnitude with quantum resistance and scattering resistance.

B. Capacitance for CNT

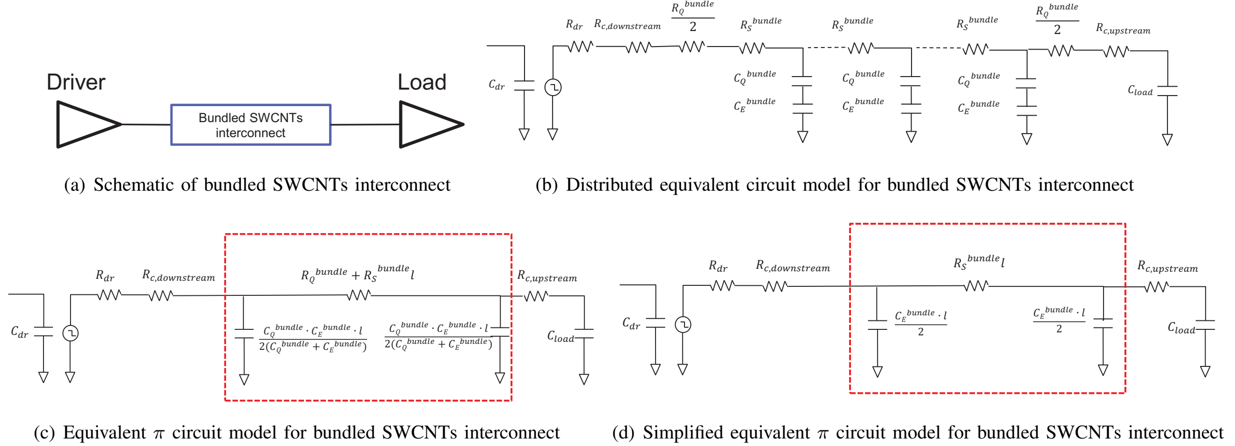
1) Capacitance for An Isolated SWCNT: The capacitance of the CNT comes from two aspects. One is the electrostatic capacitance denoted by C_E, and the other is quantum capacitance denoted by C_Q.

The quantum capacitance $C_Q l$ is obtained by [28]:

$$C_Q l = \frac{2e^2}{hv_f} l. \tag{5}$$

Since an SWCNT has four conducting channels, the net quantum capacitance of an isolated SWCNT is

$$C_Q^{CNT} l = 4C_Q l. \tag{6}$$



(a) Schematic of bundled SWCNTs interconnect

(b) Distributed equivalent circuit model for bundled SWCNTs interconnect

(c) Equivalent π circuit model for bundled SWCNTs interconnect

(d) Simplified equivalent π circuit model for bundled SWCNTs interconnect

Fig. 2. Equivalent circuit model for bundled SWCNTs interconnect [7].

The quantum capacitance for a bundled SWCNT can be computed as

$$C_Q^{bundle} l = N_{cnt} C_Q^{CNT} l. \tag{7}$$

The electrostatic capacitance C_E is calculated by treating the CNT as a thin wire, with diameter d and the distance to the ground plane y. $C_E l$ can be calculated as follows

$$C_E l = \frac{2\pi\epsilon}{cosh^{-1}(y/d)} l, \tag{8}$$

where ϵ is the permittivity of free space. The electrostatic capacitance for a bundled SWCNTs C_E^{bundle} is given by a parallel combination of all SWCNTs in the bundle. The electrostatic capacitance can be calculated using FastCap [29].

According to [7], besides quantum capacitance and electrostatic capacitance, capacitance between metallic and semi-conducting SWCNTs within a bundle is not important. In addition, the effect of the quantum capacitance is small, the effective capacitance of an SWCNTs bundle is nearly equal to its electrostatic capacitance [7].

$$C_{bundle} l = C_E^{bundle} l. \tag{9}$$

C. Inductive Impact is Not Important

According to [7], the inductive impact is not important. It shows that an RC model for interconnect delay is accurate when the following inequality does not hold.

$$R_{dr} Cl < \frac{1}{2} RlCl < \sqrt{LC} l, \tag{10}$$

where R_{dr} is the driver impedance and R, C and L are the per unit length interconnect resistance, capacitance and inductance. According to the simulation conducted in [7] for different size of driver and SWCNTs, Eq. 10 is never satisfied. Therefore, RC model is sufficient to handle bundled SWCNTs interconnect delay.

D. Elmore Delay Model for Bundled SWCNTs

This work uses the Elmore delay model for bundled SWCNTs proposed in [7]. Refer to Figure 2. The schematic of the driver, load and interconnect is shown in Figure 2(a). The interconnect is made of bundled SWCNTs. Elmore delay model for bundled SWCNTs with the driver and load capacitance is shown in Figure 2(c) which is derived from the distributed equivalent circuit model shown in Figure 2(b). R_{dr} is the resistance of the driver and C_{load} is the load capacitance connecting to the interconnect. $R_{c,downstream}$ is the contact resistance between the driver and the bundled SWCNTs interconnect and $R_{c,upstream}$ is the contact resistance between the bundled SWCNTs interconnect and load capacitance. R_Q^{bundle} and R_S^{bundle} are the quantum and scattering resistance of bundled SWCNTs, respectively. C_Q^{bundle} and C_E^{bundle} are the quantum and electrostatic capacitance of bundled SWCNTs, respectively. Since the capacitance of bundled SWCNTs is approximately equal to the quantum capacitance of the bundled SWCNTS and quantum resistance is not important for long global interconnect, the π model can be simplified to Figure 2(d).

IV. Timing Buffering For Carbon Nanotube Interconnects

Our algorithm for carbon nanotube interconnect timing driven buffer insertion problem is based on the dynamic programming algorithm in [2]. In the algorithm, a 3-tuple (Q, C, W) is used to characterize each buffering solution. Q represents the required arrival time for each buffering solution, C represents the downstream capacitance for each buffering solution, and W is the cumulative buffer cost of the buffering solution. Working under the dynamic programming framework [2], the tree is processed in a bottom-up fashion and a set of candidate buffering solutions and the corresponding 3-tuple are propagated from sinks to driver. Precisely, a routing tree is traversed by depth first search, and the calculation/propagation for Q, C, W begins when a sink is reached. The algorithm will compute Q, C and W from sinks up to driver.

Pruning is an important technique in buffer insertion technique due to its effectiveness in reducing the number of solutions. Following [2], for any two solutions denoted by γ_1, γ_2 at the same node, γ_2 is said to be inferior to γ_1 and is thus pruned if $Q(\gamma_1) \geq Q(\gamma_2)$, $C(\gamma_1) \leq C(\gamma_2)$ and $W(\gamma_1) \leq W(\gamma_2)$. In other word, one will compare two solutions with the same set of processed candidate buffer locations by their required arrival time, downstream capacitance and cumulative buffer cost.

When the solutions are propagated all the way up to the driver, one can obtain all the non-inferior solutions. The one with smallest W satisfying timing constraint will be returned.

During the dynamic programming, there are four operations, namely, add wire, add buffer, add driver and branch merge. They are described as follows.

A. Add Buffer

This operation is invoked when a buffer is to be inserted at a candidate buffer location v. In any buffering solution γ, after a buffer insertion, a new solution γ' will be generated. The cost $W(\gamma')$ will be computed as $W(\gamma') = W(\gamma) + W(b)$ if the buffer b is inserted. Refer to Figure 3. Recall that the buffer resistance is $R(b)$, buffer capacitance is $C(b)$, and buffer intrinsic delay is $t(b)$. To handle the contact resistance, recall that the contact resistance for the contact linking the buffer b with the downstream CNT wire is $R_{c,downstream}(b)$, and the contact resistance for the contact linking the upstream CNT wires with the buffer b is $R_{c,upstream}(b)$. The required arrival time needs to be updated considering the buffer delay and capacitance need to be set to the input capacitance of the buffer. Sinks can be similarly handled. We have

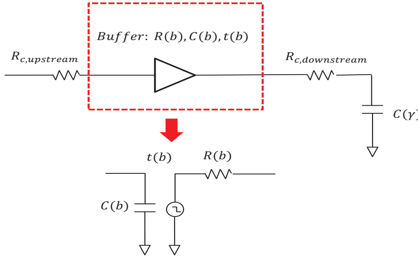


Fig. 3. Circuit and parameters for add buffer.

$$\begin{aligned} Q(\gamma') &= Q(\gamma) - R(b) \cdot C(\gamma) - R_{c,downstream}(b) \\ &\quad \cdot C(\gamma) - R_{c,upstream}(b) \cdot C(b) - t(b) \\ C(\gamma') &= C(b) \\ W(\gamma') &= W(\gamma) + W(b). \end{aligned} \tag{11}$$

B. Add Driver

This operation is to add the driver b to the candidate buffering solution. It is similar to the add buffer operation with difference that one does not compute the delay due to the upstream contact resistance of the driver and one does not update the cumulative buffer cost.

$$\begin{aligned} Q(\gamma') &= Q(\gamma) - R(b) \cdot C(\gamma) \\ &\quad - R_{c,downstream}(b) \cdot C(\gamma) - t(b) \\ C(\gamma') &= C(b) \\ W(\gamma') &= W(\gamma). \end{aligned} \tag{12}$$

C. Add Wire

Since the resistance of bundled SWCNTs global interconnect is related to the length, it can simply assumed that the distance between two consecutive buffers is larger than $1\mu m$. Under this assumption, the resistance of bundled SWCNTs can be simply $\frac{6.45k\Omega}{N_{cnt}}/\mu m$. In this operation, one is to add a wire from location v to its upstream location u for a candidate buffering solution. Recall that the capacitance for the wire (u, v) is computed as $C(u, v) = C_E^{bundle} \cdot l(u, v)$ and the resistance for the wire (u, v) is computed as $R(u, v) = R_{bundle} = R_S l(u, v)/N_{cnt}$, where $l(u, v)$ is the length of wire (u, v). We have

$$\begin{aligned} Q(\gamma_u) &= Q(\gamma_v) - R(u, v) \cdot [\frac{C(u, v)}{2} + C(\gamma_v)] \\ C(\gamma_u) &= C(\gamma_v) + C(u, v) \\ W(\gamma_u) &= W(\gamma_v). \end{aligned} \tag{13}$$

D. Branch Merge

This operation is to merge the solutions in two branches connected by a branching point. Since the solutions along each branch have been computed, one will compute the combinations among them. Suppose that there are a solution $(Q(\gamma_1), C(\gamma_1), W(\gamma_1))$ at left branch and a solution $(Q(\gamma_2), C(\gamma_2), W(\gamma_2))$ at right branch. After merging, we have

$$\begin{aligned} Q(\gamma) &= min\{Q(\gamma_1), Q(\gamma_2)\} \\ C(\gamma) &= C(\gamma_1) + C(\gamma_2) \\ W(\gamma) &= W(\gamma_1) + W(\gamma_2). \end{aligned} \tag{14}$$

That is, one needs to set the merged required arrival time to be smaller required arrival time on two branches, the total downstream capacitance to be the sum on the downstream capacitance on two branches, and the total buffer cost to be the sum of buffer costs on two branches.

V. Experimental Results

A. Experimental Setup

The proposed carbon nanotube interconnect based timing driven minimum cost buffer insertion algorithm is implemented in C language and tested on a machine with 3.40GHz Intel Pentium CPU and 3GB memory. The results of CNT buffering are compared with copper buffering. In this paper, the buffer cost is measured by buffer area.

Our buffer library consists of 10 buffer types including 5 buffers and 5 inverters. Due to the lack of industrial buffer library at 22nm technology, a buffer library of 45nm technology [30] is scaled to 22nm technology. To calculate the resistance, capacitance and intrinsic delay of different types of buffers and inverters at 22nm node, the simulation is performed using ngspice [31]. The resistance, capacitance, intrinsic delay and gate area are shown in Table II. Linear fitting is applied to obtain resistance and intrinsic delay. The capacitance of buffer is simulated using method in [32].

TABLE III

Unit resistance and capacitance (for $1\mu m$) of global interconnects with Cu and bundled SWCNTs at 22nm node.

Properties	Cu	CNT
Unit resistance (Ω)	14.50	6.45
Unit capacitance (fF)	0.16	0.16

Our experiments are performed to 500 global nets extracted from an industrial ASIC chip in an old technology. Due to the lack of industrial nets in 22nm technology, we scale wire lengths of these old technology nets to 22nm technology.

The parameters of copper and bundled SWCNTs are presented in Table III. The unit resistance and unit capacitance are for $1\mu m$. The parameters of copper are obtained from ITRS 2007 [33]. Note that the feature size predicted by ITRS 2007 is smaller than the one in the industrial 22nm technology according to [34]. We use the ITRS parameters since the resistance

TABLE II

DIFFERENT TYPES OF INVERTER AND BUFFER PARAMETERS AT 22NM NODE. (NOTE THAT THE INVERTERS IN BUF ARE DIFFERENT FROM THOSE IN INV)

	BUF_X1	BUF_X2	BUF_X4	BUF_X8	BUF_X16	INV_X1	INV_X2	INV_X4	INV_X8	INV_X16
Resistance (Ω)	2310.0	1201.0	618.9	315.5	159.6	1846.0	976.5	514.8	270.2	139.7
Capacitance(fF)	0.21	0.44	0.88	1.76	3.51	0.44	0.87	1.74	3.49	6.97
Intrinsic delay (ps)	2.93	2.91	2.87	2.87	2.87	0.59	0.62	0.61	0.61	0.61
Area (nm^2)	15197.6	30395.2	60790.4	121580.8	243161.6	10115.6	20231.2	40462.4	80924.8	161849.6

TABLE IV

TIMING CONSTRAINED MINIMUM COST BUFFERING RESULTS ON 5 REPRESENTATIVE NETS

Test cases		1	2	3	4	5
CNT w/o contact resistance	Area (nm^2)	318666.0	364162.0	222543.0	50578.0	40462.4
	# Buffers	7	5	5	3	2
	Delay (ps)	754	611	676	1019	722
CNT w/ contact resistance (100Ω)	Area (nm^2)	379359.0	424855.0	222543.0	80924.8	40462.4
	# Buffers	7	6	5	4	2
	Delay (ps)	762	599	691	927	736
Cu	Area (nm^2)	955997.0	819412.0	475433.0	202312.0	91040.4
	# Buffers	18	17	12	10	5
	Delay (ps)	766	611	702	994	870

and capacitance information of the industrial 22nm technology are not available. The parameters of bundled SWCNTs are calculated as follows. Refer to Figure 4. The cross section area of the global interconnect is set to be $33 \times 88nm^2$. For global interconnect, the resistance of a single SWCNT is approximately $6.45k\Omega/\mu m$ since the effect of quantum resistance for global interconnect is small. The impact of different number of SWCNTs in the bundle to the CNT resistance can be observed from Figure 4. If there are 1000 metallic SWCNTs in the $33 \times 88nm^2$ area, the total resistance of bundled SWCNTs is $6.45k\Omega/\mu m/1000 = 6.45\Omega/\mu m$. Note that the density of bundled SWCNTs is $1000/(33 \cdot 88) = 0.34nm^2$ which is below the maximum density $0.66nm^2$ from ITRS 2011 [35]. The unit capacitances of bundled SWCNTs and copper are set to be the same according to [7]. In this work, one considers both the ideal contact resistance and the practical contact resistance. The ideal contact resistance means no contact resistance. In the following discussion, without considering contact resistance is identical to ideal contact resistance. The practical contact resistance is set to 100Ω which is achievable according to [17].

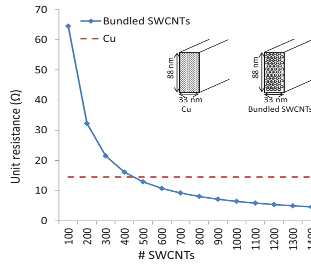


Fig. 4. Resistance comparison and cross section area of Cu and bundled SWCNTs global interconnect in 22nm technology.

B. Experimental Results

Two sets of experiments are conducted which are timing constrained minimum cost buffering and timing minimization without cost minimization, respectively.

For timing constrained minimum cost buffering, the results on five representative nets are shown in Table IV and the results on 500 nets are shown in Table V. We make the following observations.

- One can see that in order to achieve the similar delay, the CNT buffering saves more than 50% buffer area over copper buffering. Averaging over 500 nets, CNT buffering without considering contact resistance saves 58% buffer area and CNT buffering with 100Ω contact resistance saves 59% buffer area. Take net 1 in Table IV for an example, CNT buffering without considering contact resistance saves 67% buffer area and CNT buffering with 100Ω contact resistance saves 60% buffer area.
- The total number of buffers in CNT buffering is much (about $2\times$) smaller than that of copper buffering thanks to the fact that wire resistivity of bundled SWCNTs is much lower than that of copper for global interconnect as shown in Table III.
- One can see that the contact resistance does not have significant impact on the performance for CNT interconnect timing constrained minimum cost buffering.
- It would be interesting in investigating the delay-area tradeoff between copper buffering and CNT buffering. For this, net 3 in Table IV is chosen to run the buffering algorithm while keeping all non-dominated solutions. One generates delay-area tradeoff curves for copper buffering and CNT buffering, respectively. Refer to Figure 5. It is clear that CNT buffering always outperforms the copper buffering in terms of timing and buffer area.

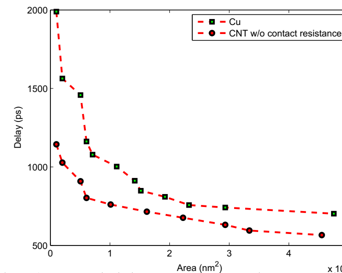


Fig. 5. Area and delay comparison between Cu and CNT.

The above results are obtained through setting certain timing constraint and compute the minimum area solutions. One may

TABLE V

AVERAGE RESULT FOR TIMING CONSTRAINED MINIMUM COST BUFFERING ON 500 NETS

Test cases	Area (nm^2)	Area ratio	# Buffers	Delay (ps)	# Solutions	CPU(s)
CNT w/o contact resistance	107816.70	0.42	3.4	1125.8	2193.2	3.79
CNT w/ contact resistance (100Ω)	105494.80	0.41	3.5	1127.9	1827.9	3.15
Cu	255110.10	1.00	7.7	1248.9	2250.0	3.54

TABLE VI

TIMING MINIMIZATION (WITHOUT CONSIDERING COST) ON 5 NETS

Test cases		1	2	3	4	5
CNT w/o contact resistance	Area (nm^2)	3307950.0	2867260.0	2477160.0	3039520.0	1945290.0
	# Buffers	50	51	44	44	32
	Delay (ps)	376	216	314	249	188
CNT w/ contact resistance (100Ω)	Area (nm^2)	1463910.0	1468890.0	1408250.0	1458970.0	1094230.0
	# Buffers	36	31	31	24	18
	Delay (ps)	423	263	347	302	229
Cu	Area (nm^2)	2851920.0	2745490.0	2269040.0	2872350.0	2142860.0
	# Buffers	65	55	56	48	36
	Delay (ps)	479	317	382	363	276

be interested in the best achievable timing in both of CNT buffering and copper buffering. The results of five representative nets for buffering timing minimization without considering cost are shown in Table VI. It demonstrates that CNT buffering can reduce timing by up to 32% which is obtained from net 5. In addition, the contact resistance has some impact on the performance of CNT buffering such as area and timing.

VI. CONCLUSION

Carbon nanotube interconnects have become a promising replacement material for copper interconnects thanks to their superior conductivity. This paper develops the first timing driven buffer insertion technique for carbon nanotube interconnects. In the experimental results, it demonstrates that with the same timing constraint, CNT buffering can save over 50% buffer area compared to copper buffering. In addition, CNT buffering can effectively reduce the delay by up to 32% without considering cost.

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