EE-2171  
Digital Logic

Curricular Designation:   CpE: required EE: required

Catalog Description:
Introduces analysis, design, and application of digital logic. Includes Boolean algebra, binary numbers, logic gates, combinational and sequential logic, storage elements, schematic and hardware-description-language based synthesis. Credits: 2.0 Lec-Rec-Lab: (2-0-0) Semesters Offered: Fall Spring Pre- requisites: CS 1121 or CS 1131

Textbooks(s) and/or Other Required Materials:

Prerequisites by Topic:
1. Familiarity with computer programming.

Course Objectives:
1. Combinational logic design including familiarity with Boolean algebraic equations and mastery of Karnaugh maps.
2. Mastery of number representation in binary, octal and hexadecimal, two’s complement addition, binary multiplication, and BCD addition.
3. Introduction to multiplexers, decoders, encoders and code converters.
4. Introduction to SR, JK, & T flip flops, familiarity with D flip flops
5. Familiarity with synchronous sequential logic design using D flip flops, including finite state machines.
6. Introduction to asynchronous sequential logic design, including races and hazards.
7. Familiarity with Verilog logic design.
Topics Covered:

1. Combinational logic design
   a. Boolean algebra, algebraic manipulation of Boolean equations with 2-3 variables, & Karnaugh maps with 4-5 variables
   b. Multiplexers, decoders, encoders and code converters
   c. Programmable logic devices, practical aspects
2. Number representation and calculations
   a. Binary, octal, hexadecimal and two’s complement
   b. Binary addition and multiplication, two’s complement and BCD addition
3. Sequential logic
   a. Latches, master-slave and edge-triggered flip flops
   b. Introduction to RS, T and JK flip flops
   c. Synchronous logic analysis and design with D flip flops
   d. Asynchronous design with simplified assignments, hazards and races
4. Logic design with Verilog

Relationship of Course to Program Outcomes (See UPAC SOP, Tables 1 and 2):

- **EE:**
  - Outcome: a via topic(s): 1a, 2a, 2b, 3
  - Outcome: c via topic(s): 1a, 3b, 3c, 4
  - Outcome: k via topic(s): 4
- **CpE:**
  - Outcome: a via topic(s): 1a, 2a, 2b, 3
  - Outcome: k via topic(s): 4
  - Outcome: n via topic(s): all
  - Outcome: p via topic(s): all
  - Outcome: s via topic(s): all

Contribution of Course to Meeting the Professional Component:

- **EE:** Engineering Topics
- **CpE:** Engineering Topics

Class/Laboratory Schedule (note: 1 hour = 50 minutes):
Lecture: 30 hours = 2 hours/week for 15 weeks

Prepared by:
Jindong Tan, Assistant Professor, June 1, 2004