EE-2304
Logic and Signals Lab

Curricular Designation:  CpE: required EE: required

Catalog Description: Experimental solution of engineering problems. Includes design, simulation, and evaluation; advanced measurement techniques in digital and signal processing systems. Credits: 1.0 Lec-Rec-Lab: (0-0-3) Semesters Offered: Fall Spring Pre-requisites: EE 2150 and EE 2171 and EE 2303

Textbooks(s) and/or Other Required Materials:
None

Prerequisites by Topic:

1. Familiarity with the spectral representation of analog and discrete sinusoids.
2. Familiarity with FIR filters and their response by convolution.
3. Familiarity with the frequency response of FIR and IIR filters.
4. Familiarity with the z-transform analysis of FIR filters.
5. Mastery of combinational logic design by Karnaugh map of 4- to 5-variable functions.
6. Familiarity with digital logic implementation technology and CAD tools.
7. Mastery of number representation in binary, octal and hexadecimal, two’s complement addition, binary multiplication, and BCD addition.
8. Introduction to multiplexers, codecs and code converters.
9. Introduction to SR, JK and T flip flops; familiarity with D flip flops.
10. Familiarity with synchronous sequential logic design using D flip flops.
11. Familiarity with asynchronous sequential logic design, including races and hazards.
12. Familiarity with Verilog Hardware Description Language.

Course Objectives:

1. Design, simulate, fabricate and test combinational and sequential logic circuits using integrated circuits and gate arrays
2. Familiarity with digital and analog interface
3. Familiarity with Verilog programming and applications
4. Familiarity with DSP applications using Matlab
Topics Covered:

1. Introduction to sequential circuits
2. Introduction to Max+ II
3. Orientation to the Altera UP-2
4. Digital to analog interface
5. Signal Generation and Wave Shaping
6. System Frequency Response
7. Filter Design with Matlab
8. DSP Applications
9. Current Topics in DSP and Digital Logic Design, Oral presentations

Relationship of Course to Program Objectives (See UPAC SOP, Tables 1 and 2):

EE:

Outcome: a via topic(s): (1-9)
Outcome: b via topic(s): (1-9)
Outcome: c via topic(s): 7
Outcome: g via topic(s): 9
Outcome: k via topic(s): (1-8)

CpE:

Outcome: a via topic(s): (1-9)
Outcome: b via topic(s): (1-9)
Outcome: c via topic(s): 7
Outcome: g via topic(s): 9
Outcome: k via topic(s): (1-8)

Contribution of Course to Meeting the Professional Component

EE: Engineering topics
CpE: Engineering Topics

Class/Laboratory Schedule (note: 1 hour = 50 minutes):
Instructional Lab: 45 hours = (1 session/week @ 2 hours/session) for 15 weeks

Prepared by: Glen Archer, Lecturer, June 1, 2004