EE-3173
Hardware/Software System Integration

Curricular Designation:  
CpE: required  
EE: Elective

Catalog Description:  
Covers the integration of hardware and software into a complete working system. Includes design and construction of I/O devices for microprocessor - or microcontroller-based systems, communication and bus protocols, programming in assembler language and in "C", system integration and testing. Also covers the use and integration of FPGAs using both schematic capture and HDL design tools. Laboratory assignments include signal-processing applications. Credits: 4.0 Lec-Rec-Lab: (0-3-2)

Semesters Offered:  
Fall Spring

Pre-requisites:  
EE 2304 and EE 3130 and CS 2141 and CS 3421

Textbooks(s) and/or Other Required Materials:

2. Relevant manuals for the hardware and software tools used in the course.
3. Specifications or other documentation relevant to the industry standards presented in the course.

Prerequisites by Topic:

1. Familiarity with programming using ANSI C, Verilog and one assembly language.
2. Familiarity with uniprocessor computer architecture, including RISC, pipelining, and I/O.
3. Familiarity with combinatorial and sequential logic designs, including laboratory practice with logic chip breadboarding, multimeters, oscilloscopes and signal generators.
4. Familiarity with synchronous sequential logic design using D flip-flops, including finite state machines.
5. Familiarity with digital logic implementation technologies such as NMOS, CMOS, TTL and FPGA, and with electronic devices such as diodes, op-amps, BJTs and MOSFETs, and associated propagation delays.

Course Objectives:

1. Familiarity and practice with System-On-a-Programmable Chip (SOPC) concepts and implementation in contemporary FPGA technology; including embedded processor cores, and selected industry standards for busses and I/O interfaces.
2. Familiarity and practice using a contemporary design tools suite for hardware and software design and integration in an SOPC environment.
3. Familiarity and practice in interfacing with a SOPC system with off-chip components, including A/D, D/A, amplification and fanout.
4. Familiarity and practice programming a processor embedded on an SOPC in both high level and assembly languages to monitor and control a real-world process, system, or device.
Topics Covered:

1. Microprocessor and microcontroller architectural issues,
2. Review and expansion on microprocessor architectures, pipelines, and I/O features
   a. Microcontroller architectures, typical I/O devices and their applications in embedded systems,
3. Principles and practice of I/O and communication including
   a. Bus signaling protocols,
   b. Programmed I/O, DMA and I/O Processors (I/O channels),
4. Selected industry communication standards, including comparative studies of at least:
   a. Two parallel system expansion busses,
   b. Two serial I/O busses,
   c. One real-time system busses and/or architectures.
5. How topics 1, 2 and (where relevant) 3 are implemented in the selected SOPC system,
6. How to use the suite of design tools for the chosen SOPC system, including hardware and software generation, integration and debugging in both high level and assembly languages.
7. Interfacing SOPC systems to external hardware, including op-amps and higher power devices.

Relationship of Course to Program Outcomes (See UPAC SOP, Tables 1 and 2):

- **EE:**
  - Outcome: a via topic(s): (all)
  - Outcome: c via topic(s): 5, 6
  - Outcome: k via topic(s): 4, 5, 6

- **CpE:**
  - Outcome: a via topic(s): (all)
  - Outcome: c via topic(s): 5, 6
  - Outcome: k via topic(s): 4, 5, 6
  - Outcome: n, r, s via topic(s): (all)
  - Outcome: q via topic(s): 5

Contribution of Course to Meeting the Professional Component

- **EE:** Engineering Topics.
- **CpE:** Engineering Topics.

Class/Laboratory Schedule (note: 1 hour = 50 minutes):

Lecture: 45 hours = 3 hours/week for 15 weeks
Lab: 26 hours = 2 hours/week for 13 weeks

Prepared by:

Brian T. Davis, Assistant Professor, May 21, 2004.