

EE-4271 VLSI Design

Curricular Designation: CpE: Elective EE: Elective

Catalog Description: Design of VLSI circuits using CAD tools. Analysis of physical factors affecting performance. *Credits:* 4.0 *Lec-Rec-Lab:* (0-3-2) *Semesters Offered:* Fall Summer *Prerequisites:* EE2171 and EE3130

Textbooks(s) and/or Other Required Materials:

1. Douglas Pucknell & Kamran Eshraghian, *Basic VLSI Design*, Prentice Hall, 1994. OR
Sung-Mo Kang & Yusuf Leblebici, *CMOS Digital Integrated Circuits*, McGraw Hill, 1999
2. John P. Uyemura, *Physical Design of CMOS ICs Using L-Edit*, PWS Publishing, 1995.
3. Relevant manuals for software tools used in the course.

Prerequisites by Topic:

1. Familiarity with the operation of MOSFETs, digital logic gates and complex logic circuits.
2. Familiarity with circuit simulation and analysis using P-Spice.

Course Objectives:

1. Familiarity with CMOS Circuits, their fabrication and modeling and with VLSI chip design issues.
2. Mastery of designing CMOS circuits using a CAD tool such as L-Edit.
3. Application of a CAD tool such as P-Spice for the simulation and analysis of CMOS circuits.

Topics Covered:

1. Introduction to a VLSI design tool called L-Edit
2. CMOS fabrication and layout, lithography, fabrication sequence, design rules
3. Modeling of CMOS Circuits, n-FET, p-FET, inverter, SPICE models, latch-up
4. CMOS Circuits, NAND, NOR, XOR and XNOR gates, AOI and OAI gates, complex CMOS circuits
5. VLSI Chip Design Issues, cells and hierarchy, floorplan, interconnects, power distribution
6. Introduction to VHDL
7. Application of L-Edit to designing CMOS circuits of varying complexity such as an inverter, 2-input NAND gate, 2-input NOR gate, 3-input NOR gate, XOR and XNOR gates, 4-bit parallel adder, etc.

Relationship of Course to Program Outcomes (See UPAC SOP, Tables 1 and 2):

- **EE:** Outcome: a via topic(s): 3, 5, 6
Outcome: c via topic(s): 1, 2, 4, 5, 6, 7
Outcome: m via topic(s): 7
- **CpE:** Outcome: a via topic(s): 3, 5, 6
Outcome: c via topic(s): 1, 2, 4, 5, 6, 7
Outcome: k via topic(s): 7

Contribution of Course to Meeting the Professional Component:

- **EE:** Engineering Topics
- **CpE:** Engineering Topics

Class/Laboratory Schedule (note: 1 hour = 50 minutes):

Lecture: 30 hours = 2 hours/week for 15 weeks

Directed VLSI design: 15 hours = 1 hour/week for 15 weeks

Lab: 30 hours = 2 hours/week for 15 weeks

Prepared by:

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