Choose six (6) of the eight (8) questions you wish to be graded by circling the question numbers. If more than six (6) questions are circled, only the first six (6) circled questions will be graded.
1. The switch closes at $t = 0$. $R_1 = R_2 = 1\, \Omega$, $C = 1\, \text{F}$. Assume zero initial conditions. Find the capacitor voltage $v_c(t)$, $t \geq 0$. 

![Circuit Diagram]

10V

$\text{R}_1$

$\text{R}_2$

$C$

$V_c$

$+$

$-$
2. Let \( u(t) \) be the unit step function.

(a) \( f(t) \) is a signal. Write down the definition of its Laplace transform \( F(s) \).

(b) For the signal \( f(t) = e^{-at}u(t) \), calculate its Laplace transform \( F(s) \) and find its region of convergence (provide details).

(c) For the signal \( g(t) = e^{at}u(-t) \), calculate its Laplace transform \( G(s) \) and find its region of convergence (provide details).
3. Consider a 5-bit “majority detector” logic function. In this function, we always want the output of the circuit to reflect the most common value that is currently being inputted to the function. For example, if the five inputs are \{1, 1, 0, 0, 0\}, the output of the circuit should be 0. Answer the following questions about this function.

(a) Complete a truth table for this circuit that exhaustively defines the behavior.

(b) Using the minimization method of your choice, find a minimal Sum of Products form of the function.

(c) Use Verilog (or another hardware description language of your choice) to express the behavior of the “majority detector”. Your answer may directly proceed from your work in part 2 or may be all-new work.
4. Input voltage waveform \( v_I \) shown below is applied to each of the three ideal op-amp circuits also shown below. For each circuit, derive an expression for the output voltage \( v_o(t) \) and then plot it as accurately as you can.

(a)
5. Find the output of the system shown below

\[
x(t) \xrightarrow{h(t)} y(t)
\]

with the impulse response

\[
h(t) = \begin{cases} 
2 & 1 \leq t \leq 3 \\
0 & \text{else}
\end{cases}
\]  \hspace{1cm} (1)

and the input \( x(t) = e^{-2t} u(t) \).

\[
y(t) = \]


6. We are writing a software simulation of a DMA (Direct Memory Access) Controller. The simulator should take the form of a high-level language (C/C++/Java, etc.) description of the behavior of the DMAC. Write a function that takes some kind of data structure as an input, where the data structure encapsulates all the information a DMA Controller would need in order to process a DMA request. Then, according to the data in the structure, the function should describe the actions taken by the DMA Controller in order to complete the request. Do not worry about 100% correct syntax; rather, focus on the behavior of the controller as it performs the DMA request. You are granted much freedom in the implementation and may make any design decisions you feel appropriate to complete the task. State any major assumptions or design decisions you make.
7. Regarding Hazards between instructions:
   (a) For each of the following pairs of Register-to-Register instructions, indicate what type of data hazard is involved (RAW, WAR, or WAW). Note: for a given pair, there may be more than one hazard.
   (i) \( R1 = R2 \times R3, R4 = R1 + R3 \)
   (ii) \( R1 = R2 \times R3, R2 = R1 + R3 \)
   (iii) \( R1 = R2 \times R3, R1 = R2 + R4 \)
   (b) The following types of hazards have been defined: Structural, Control-Flow, Real Data & False Data. Which type(s) of hazard(s) are either eliminated or mitigated by each of the following methods?
   (i) Data Forwarding
   (ii) Register Renaming
   (iii) Instruction Shelving (Reservation Stations)
   (iv) Branch Prediction
   (v) Pipelining an Execution Unit (e.g. a multiplier)
8. The three classes of cache misses are often referred to as the “Three Cs” (Capacity, Conflict, and Compulsory). Describe:
(a) the origins of each class, and
(b) what (if anything) can be done to ameliorate the impact of each one.